Development of Radio Frequency Circuit Using Silicon-on-Sapphire (SOS) Technology

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The Silicon-on-Sapphire (SOS) technology is used to form a source, channel and drain of CMOS on the surface of sapphire[1]. There are two aspects of SOS technology that do not exist with CMOS on silicon substrates. The first is that there is no parasitic capacitance in the source-to-ground and drain-to-ground segments of transistors. When ordinary circuits are implemented on silicon substrates, the sources and drains of transistors are individually connected to the substrate via their junction capacitors. A portion of the electrical power from high frequency signals that pass through these sources and drains is leaked to the ground through the substrate. When SOS is used, however, high frequency signals do not lose any electrical power through the substrate. Furthermore, signals are not leaked from sources to drains via the substrate when the transistor is turned off, providing superior insulation characteristics for transistors. The other aspect of SOS is that the magnetic field on the substrate does not decay from eddy currents on the substrate when an inductor is formed on the SOS. Since sapphire is insulative, eddy currents do not occur within the substrate, which means that there is much less loss of electric power by inductors. The fact that there is no parasitic capacitance with transistors on SOS and no eddy currents occur with inductors on SOS is advantageous for inhibiting the loss of electric power when designing radio frequency circuits.

During the initial phase of research of the SOS, the lattice defects captured carriers of transistors, which resulted in the deterioration of transistor characteristics, making SOS unsuitable for the fabrication of circuits. The capturing of carriers occurred at the hetero interfaces between the silicon and sapphire or in the lattice defects inside the epitaxial silicon. Since then, lattice defects in the epitaxial layer were reduced by the advancement of a crystal growth technology[2]. Furthermore, the flatness and cleanliness of the sapphire surfaces are improved due to the recent demand of substrates for blue lasers, resulting in a reduction of hetero interface defects. Supported by such technological advances, the crystallinity of the channel segment of the SOS improved to a point where it is conceivable to fabricate circuits using this technology. This paper will introduce an example of the development of radio frequency circuits using SOS and then describe features of the SOS technology.

Antenna Switch

An antenna switch illustrates quite dramatically a feature of the SOS, namely the quite small amount of signal loss when high frequency signals pass through the sources and drains of transistors. The intended uses and required performance of antenna switches, as well as characteristics of antenna switches fabricated on top of SOS substrates are described in this section.

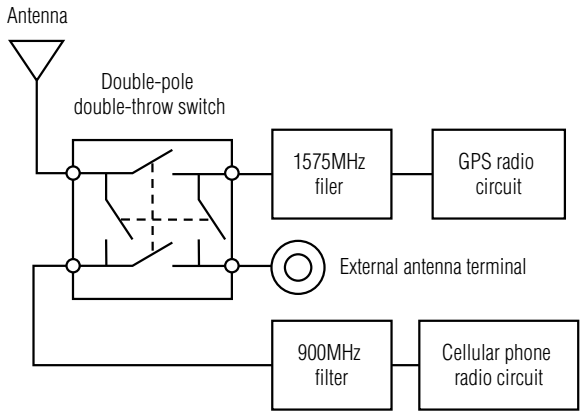

Fig. 1 An example of usage of antenna switch

Due to the multifunctional evolution of cellular phones, individual terminals are transmitting and receiving multiple signals that are different in terms of frequencies, as well as signal standards. Illustrated in **Figure 1** is an example of a cellular phone terminal, which has a built-in global positioning system (GPS). The frequency of cellular phones may, for example, be 900MHz, while the frequency of GPS is 1575MHz. Multiple integrated circuits suitable for individual radio frequencies are loaded into these phones. Each of these integrated circuits is connected to the antenna for various frequencies via band pass filters. A switch must then be installed between the antenna and the filters.

Since this switch is needed for the distribution of radio waves of varying standards to individual radio integrated circuits, strict values are required with regards to insertion losses and isolation characteristics. Because signals pass through the sources and drains of switch transistors, the low amount of electric power loss with SOS means there will be a reduction in insertion losses.

The characteristics of a double-pole double-throw (DPDT) switch developed with the SOS technology is shown in **Table 1**. The fabrication of this switch was conducted using the 0.5μm SOS-CMOS process. The opening and closing of the switch is performed by choosing either of the two conditions shown in **Figure 2** through the selection of a control terminal voltage. The control terminal is abbreviated in **Figure 2**.

Table 1 Characteristics of antenna switch

Insertion loss	900MHz 1900MHz	0.5dB 0.7dB
Isolation	900MHz 1900MHz	20dB 14dB
Reflection loss		-20dB
Harmonic generation		-75dBc
IIP3	900MHz 1900MHz	60dBm 60dBm
Power source voltage		3V
Power source current		15μA

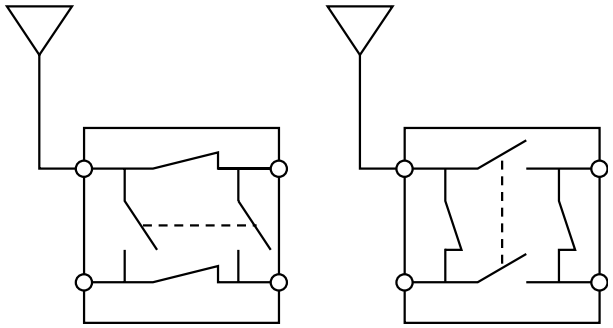

Fig. 2 Switching action of double-pole double-throw antenna switch

The figure of the insertion loss, 0.7dB, is equivalent to figures obtained with switches that are manufactured with compound semiconductors and is a true indication of the insulative characteristics of sapphire substrates. The amount of electric power that can be input to the switch exceeds 3.5W and the switch, therefore, is adequately capable of withstanding the transmission electrical power of cellular phones.

Radio Reception Integrated Circuit

As already described, a feature of SOS is that the Q-factor of the inductor is high. The Q-factor is defined by dividing the amount of energy stored by oscillating elements of one cycle with the energy dissipated in one cycle. As for inductors on integrated circuits, the Q-factor becomes larger with a smaller dissipation of electric power by the substrate. Inductors are used on radio integrated circuits for the purpose of impedance matching of the input and output for amplifiers, providing the load for amplifiers and in the LC resonance segments of oscillators. Shown is the characteristic when the Q-factor is higher, the frequency selectivity for impedance matching is enhanced, gains of amplifiers are higher and the spectrum of resonators is more acute.

If we were to assume that the main cause of electric power loss is the series resistors, then the Q-factor of inductors can be obtained by the equation, $Q=\omega L/R$, where ω is the angular frequency of the signal applied to the inductor, L is the inductance and R is the series resistor of the inductor. In order to increase the Q-factor, under ideal conditions, only the wiring widths of inductors would need to be broadened and the resistance of series resistors reduced. In reality, however, since an eddy current occurs in the silicon substrate, the broadening of wiring lines increases decay because of the eddy current and the Q-factor can only be increased to about 10[3]. If the substrate is made of sapphire, however, there is no generation of an eddy current since sapphire is insulative and by broadening the wiring width, the Q-factor can be increased up to about 30.

Taking notice of the characteristics of inductors mounted on the SOS, we fabricated a radio reception integrated circuit for the global positioning system using the SOS technology. A block of a radio frequency segment from a radio reception integrated circuit is shown in **Figure 3**. The fabrication was carried out using the 0.25μm SOS-CMOS process. There are two variations of n-type MOS transistors, those with a threshold value of 0V and those of 0.7V. Both of these variations were used in the circuit design.

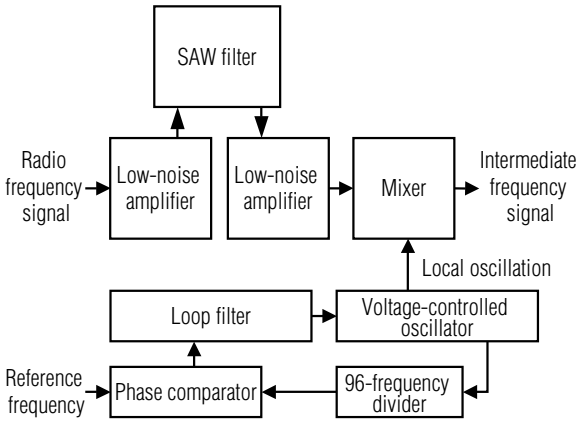

Fig. 3 Global positioning system receiver developed using the SOS technology
(The figure only shows the radio frequency segment of the circuit.)

The radio wave received from satellites of the global positioning system (1575.420MHz) is quite faint, less than only 1pW. The low-noise amplifier of the first stage amplifies the radio wave, while sustaining the signal to noise ratio as much as possible. This means that the noise figure of the amplifier is required to be small. The signal is amplified by the low-noise amplifier of the first stage, then the frequency of 1575.420MHz is selected by the surface acoustic wave (SAW) filter mounted externally on the integrated circuit and then amplified again by the low-noise amplifier of the second stage. At this point, the electric power of the received signal is adequately larger than the thermal noise and the signal to noise ratio is not affected very much by the thermal noise generated by the circuit in the latter stages. The signal amplified with the carrier frequency of 1575.420MHz is converted to an intermediate frequency of 4.092MHz by the mixer, which takes the difference between the signal that has been amplified and the frequency from local oscillation (with a frequency of 1571.328MHz). The local oscillation is generated by the voltage-controlled oscillator and phase-locked loop (composed of a 96-frequency divider, phase comparator and loop filter). The integrated circuit also has an intermediate frequency circuit which consists of a band

pass filter and limiter amplifier, however, it is abbreviated in **Figure 3**.

In the following section this paper focuses on the low-noise amplifier of the first stage and voltage-controlled oscillator from the block shown in **Figure 3** and describes their characteristics.

(1) Low-noise amplifier

Characteristics of a low-noise amplifier of the first stage are shown in **Table 2**. The circuit is a single-ended circuit with cascaded source grounding[4]. The inductor is used for the input impedance matching and as a load for transistors.

Table 2 Characteristics of low-noise amplifier

Center frequency	1575MHz
Gain	16-20dB
Noise figure	2.5dB
Isolation	25dB
Reflection loss	-10dB
IIP3	-14dBm
Power source voltage	1.5V
Power source current	1.0-2.0mA

The low-noise amplifier exhibits a gain of 16dB and a noise figure of 2.5dB with a power consumption of 3.0mW. The gain can be increased up to 20dB using the regulating function. This gain is adequate for an amplifier of the first stage while the electric power consumption is low due to the low electric power loss characteristics of transistors and inductors. The noise figure of low-noise amplifiers mounted on silicon substrates increases as the electric power dissipation from the input signal pad to the silicon substrate reduces the gain[5]. In the case of SOS, however, the amplifier indicates an adequate gain and a reasonable noise figure, because the parasitic capacitance of the pad may be ignored, even when electrostatic discharge protection elements are connected to the input terminals of low-noise amplifiers. The IIP3 (the third input interceptor point) is -14dBm, which is a relatively large figure and, in spite of the low electric voltage, 1.5V, there is an adequate wave formation between the input and output of electric power.

Since the low-noise amplifier is connected to the antenna for input and to the SAW filter for output, the input and output impedance must be 50Ω. The matching circuit for 50Ω is located inside the integrated circuit and there is no need to add any external matching components. An inductance greater than 10nH is usually required to match the input impedance for the frequency of global positioning systems (1575MHz). Integration is difficult with silicon substrates, since fabricating a large inductance increases the number of series resistors in the wiring and the amount of parasitic capacitance due to an increased number of coils, which results in increased amounts of eddy current loss of the substrate. Due to the characteristics of SOS, however, a large inductance of 18nH with a Q-factor of 16 can be used with this low-noise amplifier, enabling the matching of impedance in the integrated circuit.

(2) Voltage-controlled oscillator

Characteristics of the voltage-controlled oscillator are shown in **Table 3**. The circuit is composed of the CMOS negative resistor, inductor, n-MOS variable capacitor, as well as a buffer that drives the frequency divider and mixer. The inductor has an inductance of 3.7nH with a Q-factor of 15.

Table 3 Characteristics of a voltage-controlled oscillator

Oscillation frequency	1440-1880MHz
Phase noise	-114dBc/Hz (1MHz)
Power source voltage	1.5V
Power source current	1.4mA

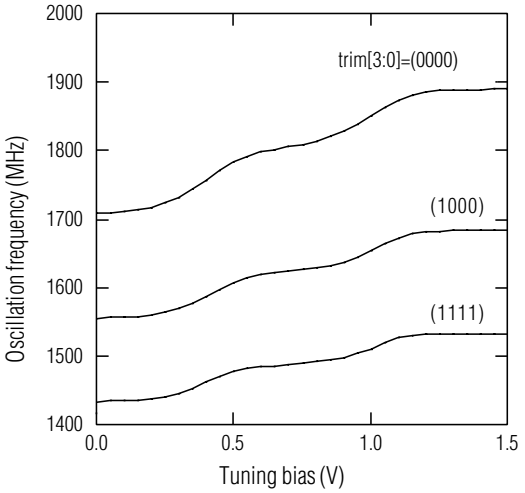

Fig. 4 Oscillation frequency of voltage-controlled oscillator

The oscillator operates with a direct current electric power consumption of 2.1mW. The amount of electric power consumed by the buffer is also included in this figure, so the electric power consumption is low for the entire oscillator. The oscillation frequency is in the range of 1440 to 1880MHz, which is switched by changing the trimming capacitance and control terminal voltage, as shown in **Figure 4**. The trimming capacitance is a means to compensate for the fluctuation of the oscillation frequency arising from irregularities in the manufacture of transistors and the optimum capacitance value is selected automatically when the integrated circuit is turned on. **Figure 4** indicates that the oscillation frequency varies greatly when the proximity of the control voltage is 0.5V and 1.0V. This is due to the fact that two types of MOS capacitors with different threshold values were used for variable capacitors. A frequency lock is applied by the phase-locked loop on the oscillation frequency, resulting in a spectrum for the intermediate frequency, as shown in **Figure 5**.

The phase noise is -119 to -114dBc/Hz for an offset frequency of 1MHz. The primary source of phase noise is understood to be the flicker noise of transistors, based on the spectrum analysis. Flicker noise is generated by lattice defects in the channel or when electron levels in the hetero interface captures or discharges carriers[6]. In the case of SOS, the existence of misfit dislocations of

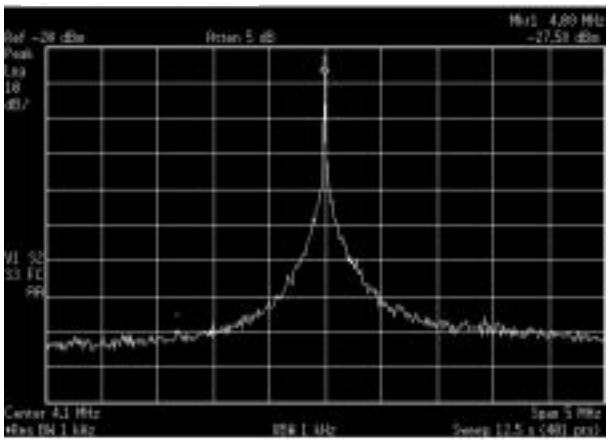

Fig. 5 Spectrum of intermediate frequency with phase-locked loop

the hetero interface between sapphire and silicon is unavoidable. The threading dislocation in the silicon layer is reduced during the solid phase growth of silicon, but it is not completely eliminated. Furthermore, the number of defects remaining after the solid phase growth is comparatively higher than with bulk. In order to reduce the phase noise of a voltage-controlled oscillator with SOS, aside from contriving devices in the circuitry, it is important to bring up the crystalline characteristics of the silicon layer on the sapphire to a level of bulk and reduce the electron level in the transistor channel.

Conclusion

An antenna switch, as well as a low-noise amplifier and voltage-controlled oscillator were introduced as silicon-on-sapphire (SOS) development examples of radio frequency circuits. These circuits have low levels of electric power loss, due to the characteristics of the SOS technology, which is a lack of parasitic capacitance in the source-to-ground segment of transistors and the characteristic of the large Q-factor of the inductor. Future development is expected with regards to the small amount of electric power loss in the SOS circuit, since the differentiation of the circuit from those on silicon substrates in this aspect is considered to become more prominent with higher radio frequencies handled by the circuit.

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