Time Code Receiver LSI for Radio Clocks Offer High Sensitivity and Low Electric Current Consumption Using SOI

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The number of radio clock users is on the rise because they are accurate to the second and setting the time manually is no longer necessary once a battery is installed.

The mechanism of radio clocks is such that the displayed time is automatically corrected once it receives a longwave standard frequency, superimposed by time-signal emissions in an AM modulation with the current time's real-time information ("time code"), which is transmitted by the Communications Research Laboratory[1], an independent administrative institution, from their stations in Fukushima prefecture (40kHz) and Saga prefecture (60kHz).

Because of the fact that there are only two stations in Japan and only a handful of stations overseas that transmit standard frequency, the radio clocks must be highly sensitive to be able to receive very weak radio waves with a time code receiver LSI installed inside them. As a solution, many such devices adopted the bipolar technology. The locations of the longwave standard frequency transmitting stations are shown in Figure 1.

The operating current consumption of the conventional bipolar time code receiver LSIs, was a few hundred μA. Oki Electric successfully developed a time code receiver LSI, the ML6190A, which can sustain a high level of sensitivity, comparable to conventional products, while offering an electric current consumption that has been drastically reduced to 20μA (typical), through the use of the fully-depleted-type silicon on insulator CMOS (FDSOI-CMOS) process. This paper describes the circuit configuration and future product developments of the ML6190A, and introduces examples of radio clock applications that are expected in the future.

Overview of the longwave standard frequency and time code receiver LSI functions

The longwave standard frequency, being transmitted by the Communications Research Institute, is also used as the source for the frequency standard, and for this reason it is in the form of an AM modulated wave with a modulation range of 90% (the magnitude ratio of the high and low amplitude is 10:1). The time code is coded with a pulse width, and configured by three values, the marker signal, the "1" signal, and the "0" signal. The high amplitude condition is represented by 0.2 seconds of the marker signal, 0.5 seconds of the "1" signal, and 0.8 seconds of the "0" signal. The pulse transmission rate is one bit per second, with the remainder of each second being the low amplitude condition. The code line (sequence) of the time code starts with a marker signal, followed by bit signals representing the minute, hour, aggregated total number of days since January 1, calendar year (two last digits), day of week, and marker signals inserted every ten bits, making a total length of 60 bits. A configuration of the time code is shown in Figure 2.

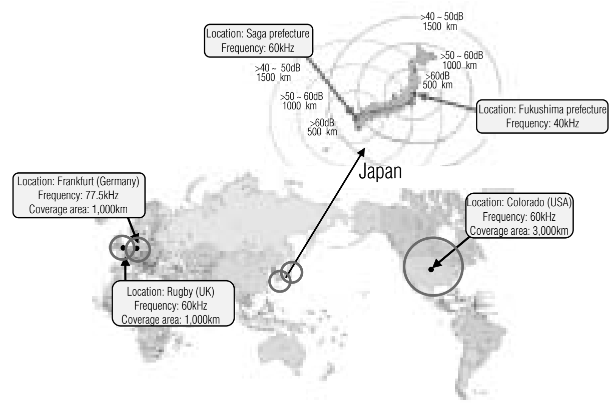

Fig. 1 Locations of the longwavestandard frequency transmitting stations

The time code receiver LSI receives and demodulates the longwave standard frequency, and outputs logical level signals with a time width that corresponds to the time width of the high amplitude of the marker signal, the "1" signal, and the "0" signal. In order for the microprocessor to identify time information from these three signal values, the time width logical signal output of the time code receiver LSI, needs to be put through a decoding process.

The importance of lowering the amount of electrical current consumed by time code receiver LSIs

Radio clocks normally require at least a few minutes or up to ten minutes to receive time codes that run over several frames, in order to carry out time corrections, as well as time code conformity verifications. Several time correction processes[2] are also performed several times a day to ensure an accurate time correction.

Although the electric current consumption of microprocessors for clocks and watches reaches a low-level electric current of approximately 1μA, the time code receiver LSI consumes a large amount of electric current when it operates. For this reason, the LSI is equipped with a power saving mode, which keeps it in a standby mode until the time information has been received. It will then enter an operating mode to identify the time code,

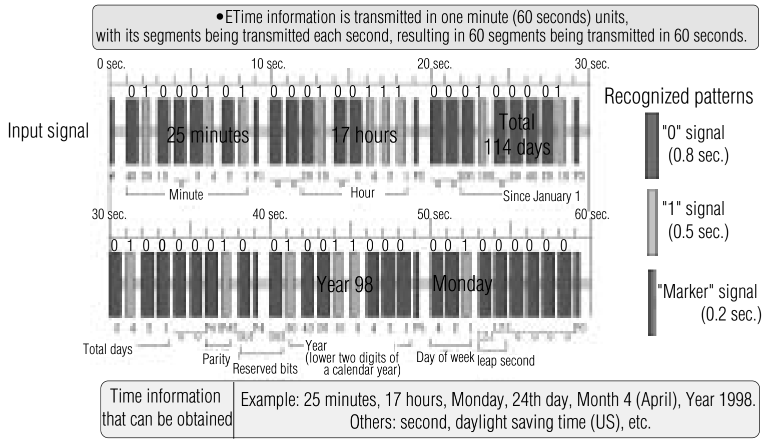

Fig. 2 Configuration of the time code

apply the appropriate correction to the display time, and resume the standby mode again. Further, since the standby times are much longer than operating times, it is also necessary to consider lowering the electric current consumption when it is in the standby mode, to reduce the overall electric current consumption.

Electrical current consumption reduction with the SOI technology

In order to reduce the current consumption of a transistor amplifier with a resistance load, it is necessary to increase the resistance load in a reverse proportion to that of the reduction of the operating current. When the time constant of the resistance load and the parasitic capacitance of the amplifier transistor becomes large, the frequency band on the high-pass will become restricted.

The junction capacitance that is the parasitic capacitance of the MOS transistor, is proportional to the junction area, and the junction area is the sum of the flat surface segment and side surface of the diffusion layer of the source and drain. With FDSOI-CMOS devices, the capacity is small, being only approximately one-tenth that of conventional bulk MOS transistors because the bottom segment of the MOS transistor is in contact with a thick oxide film (embedded oxide film). This makes it possible to greatly alleviate the restrictions on the frequency band due to the raised resistance load of the amplifier.

A precipitous lower threshold characteristic can be named as a feature of the FDSOI-CMOS. Due to this characteristic the threshold voltage can be set low, making it possible to realize low voltage operations as long as the OFF leakage current remains constant. Further, with the same threshold voltage, the OFF leakage current can be inhibited[3].

The under surfaces of transistors in FDSOI-CMOS devices, are insulated with a thick oxide film. Individual elements are isolated from each other, making it possible to block out feedback from the substrate or the intrusion of noise. Further, due to the small OFF leakage current and electric current consumption, the generation of electric current thermal noise is minimal, making it possible to achieve low noise levels.

The FDSOI-CMOS process with the aforementioned features has been adopted for the ML6190A.

Configuration and operation of the time code receiver LSI

A block diagram of the ML6190A is shown in Figure 3. The ML6190A receives a longwave standard frequency with a tuning bar antenna then it amplifies the signal to the required level with the automatic gain control (AGC) amplifier. The necessary band frequency signals are then extracted through the use of a narrow band frequency band pass filter of approximately ±5Hz using a crystal oscillator. The time code logical signal is output by the demodulation of the AM signals with the rectifier circuitry, then level conversions are performed through a comparison between the demodulated output and the reference level in the decoder circuitry. The connection capacitance of the DET (envelope DETect) terminal regulates the output envelope of the AM demodulation output.

The AGC amplifier performs amplification by adjusting the gain while maintaining the amplitude of the AM waveform that was output from the narrow band frequency band pass filter. The connection capacitance of the AGC terminal regulates the AGC time constant.

Further, although it is not shown in a block diagram, it is possible to adapt the device to operate within a broad voltage range (1.1V to 3.6V). This can be done by supplying constant voltage to the aforementioned individual circuits via a regulator circuit that has an operating mode control terminal controlling the switching between the operation and standby circuitries.

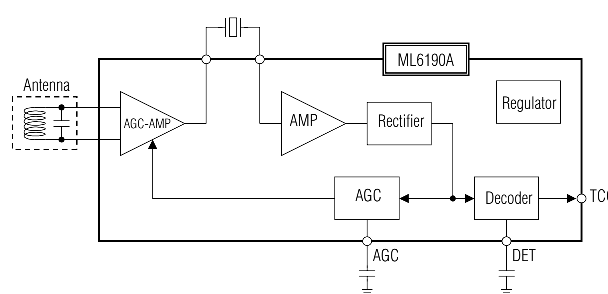

Fig. 3 Block diagram of the ML6190A

AGC circuit of the time code receiver LSI

Limited amplification can be used for the reception of FM modulated signals that have no information along the width of the amplitudes. In order to sustain information of AM modulated signals along the width of the amplitude, however, AGC amplification is needed.

Even though both the high amplitude and low amplitude conditions are always occurring every second, with the longwave standard frequencies, the time ratio of these high and low amplitude conditions are not constant, which means the AGC is more suitable, as it sustains the peak level of the high amplitude condition at a constant level.

As with the AGC that sustains a peak level of the high amplitude condition at a constant value, the amplitude levels are matched to prescribed values for the low amplitude condition as well, and so the AGC amplified waveform for the low amplitude gradually becomes larger. Because of this, the level of the envelope demodulation output also becomes larger. When this demodulated output level exceeds the comparator reference level, then the time code logical output will be inverted, resulting in an error output corresponding to the high amplitude condition. For the reception of the marker signal, the low amplitude condition becomes a long signal that lasts 0.8 seconds. In order to prevent an error in the time code logical output, it is essential that the AGC time constant be set to a value that is adequately larger than 0.8 seconds. However, if the AGC time constant is set to a large value, when the peak level of the high amplitude changes for some reason, then the recovery time to reach a stable receiver condition sometimes takes a long time.

Therefore, the time code receiver LSI seems to have contradicting requirements for setting an adequately large AGC time constant to ensure accurate demodulation of long signals that last 0.8 seconds in low amplitude conditions, but on the other hand a small AGC time constant is required to reduce the time it takes to return to the stable receiver condition after a peak level change in the high amplitude condition.

AGC circuit of the ML6190A

An AGC circuit was developed and adopted for the ML6190A that can satisfy both contradicting requirements of a reduced transition time from its power-on to stable operation condition, to its stable operations, during long low amplitude inputs.

When the ML6190A is changed from the standby mode to the operating mode by changing the control input from the operating condition control terminal, the AGC amplifier will start to operate with a maximum gain. When a longwave standard frequency is received in this condition, an excessive input condition will arise with the AGC amplifier, and the demodulated output, resulting from the demodulation of such an output, will constantly exceed the comparator reference level, and put the time code output (TCO) into the high amplitude condition consecutively.

The AGC, which sustains a constant peak level, will continue to operate while the time code output is in a high amplitude condition. The gain of the AGC amplifier rapidly decreases, to reach a stable receiver condition. Later, when the time code output changes to a low amplitude input condition, the immediately preceding AGC amplifier gain condition will be sustained.

This gain protective function keeps the time code output in a stable, low amplitude input condition regardless of the time length for the low amplitude input condition. Because of this, the AGC capacitance value needs to focus only on AGC operations to constantly maintain a peak level in the high amplitude input condition, making it possible to minimize the capacitance value, and reduce the amount of time required to transfer from the power-on to the stable receiver condition.

Future product developments

A low voltage operation and low electric current consumption was achieved, making it possible to vastly extend the battery life because the FDSOI-CMOS process, rather than the bipolar process, was adopted for the development of the ML6190A. Further, although in the past, several LSIs, including the time code receiver LSI, the time code decoder LSI (for decoding logical level signals output by the time code receiver LSI) and a microprocessor, were required. By integrating the time code receiver circuitry and various logic circuitries into a single chip without using any special processes, it is now possible to reduce the mounting surface area and costs.

Our radio clock product developments for the future are shown in Figure 4. We have completed the development of the ML6190A and in the future we shall focus our developments on theML6191, which integrates the demodulation and time code decoding circuits, while the ML6192 integrates a driver for displaying time on the ML6101. Other than these developments it is also possible to offer customized LSIs for various applications, because integration of the CPU and various logic circuits is achievable.

Scope of radio clock applications

In the past, the majority of applications for radio clocks included time keeping devices, which were represented by wristwatches and clocks. Since equipment that utilizes radio clocks have the benefit of not needing any initial settings or correction of time, radio clocks can be applied to a variety of applications.

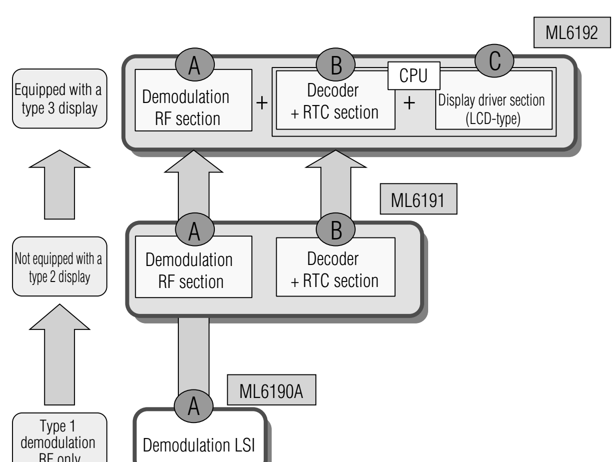

Fig. 4 Future product development of LSIs for radio clocks

Many electrical appliances developed in recent years contain clocks and timers. It is therefore, believed that the need for radio clocks will continue to rise in the future. Many products exist in which radio clocks can be used, such as AV equipment, which includes stereo sets and minicomponent stereo sets, mobile phones, digital still cameras, and video cameras; household appliances, including rice cookers and remote control units; office equipment, including copiers, fax machines, cash registers, time recorders; and equipment using late night power supplies, such as car locks and electric water heaters. Further, with the progress of electronic commerce, the accuracy of the time used between computers is becoming more important, and the effectiveness of radio clocks with a time correcting function will increase further in the field of security.

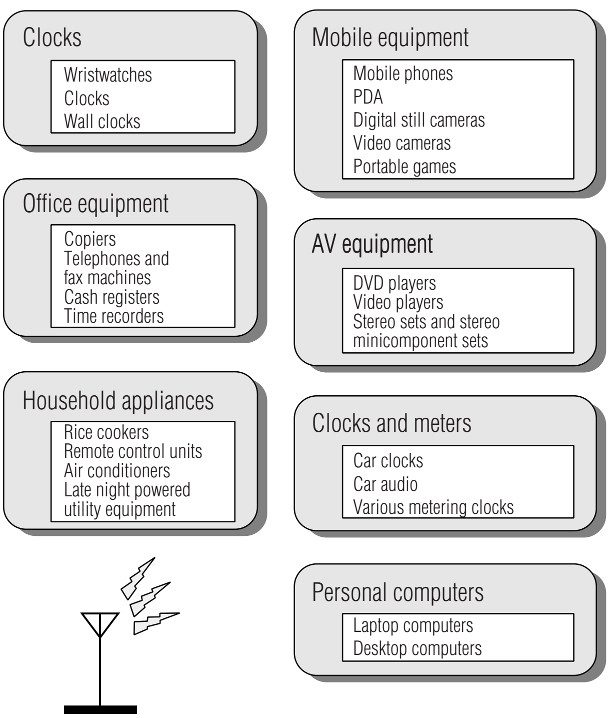

Fig. 5 Example application of radio clocks

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