GaAs IC set for optical transmission module

--From 10 Gb/s to 40 Gb/s--

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High speed and low power consumption are vital in ICs for high-speed optical communications systems. Some of the competing IC elements in this field include: Si-BJT (Silicon Bipolar Transistor), Si-CMOS (Silicon Field Effect Transistor), SiGe-BJT (Silicon Germanium Bipolar Transistor), GaAs-HBT (Gallium Arsenide Heterobipolar Transistor), GaAs-FET (Gallium Arsenide Field Effect Transistor), and GaAs-HEMT (Gallium Arsenide High Electron Mobility Transistor), amongst others. Fig. 1 shows the range of bit rates covered by these various devices, and it shows that the compound semiconductor, such as GaAs, is generally more suitable as a material for high-speed operation than Si.

The reason for this is that the electron velocity travelling in the compound semiconductor, such as GaAs, is higher than that in Si. Around 1990, prior to any of our competitors, our department at Oki started to concentrate on the development of high-speed GaAs FET and HEMT device technology as well as applying this technology to digital and analogue ICs for optical modules used in 10 Gb/s optical communications systems (STM64 or OC-192).

The front end module of an optical transmission system converts between optical signals and electrical signals, and as shown in Fig. 2, the transceiver consists of LD (laser diode), EA (electro-absorption) modulator, and modulator driver, whilst the receiver consists of PD (photo-diode), transimpedance amp, and limiting amp.[1)]

IC for transceiver

(1) 10 Gb/s EA modulator driver

The configuration for modulating (on and off) a laser

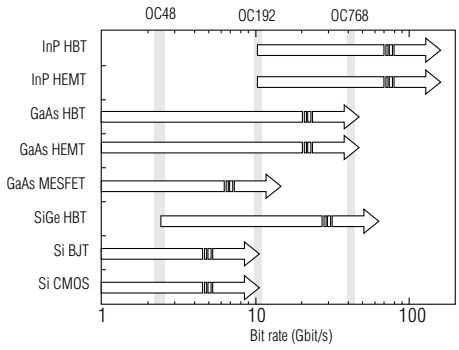

Fig. 1 Comparison of performance of different device types

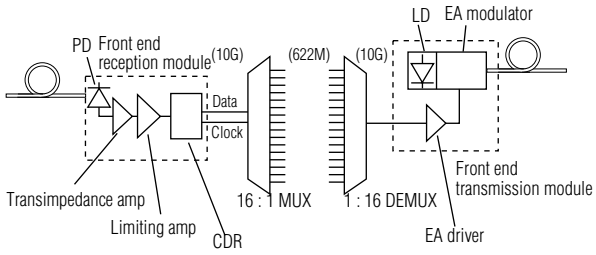

Fig. 2 Block diagram of 10 Gb/s optical transmission system

diode by directly connected driver IC is simple, but at high-speed operation exceeding 10 Gb/s, the semiconductor laser is not able to keep up sufficiently, and a problem of optical waveform distortion may occur. Therefore, this method is used principally in short-distance transmission systems (where waveform quality is not so important), but in long-haul WDM transmission systems where the quality of the optical waveform is essential, it is more common to use an external modulator, which is separate from the semiconductor laser, driven by a driver IC. Typically, the external modulator is a lithium niobate ($LiNbO_3$) Mach-Zehnder type modulator (hereinafter, "LN modulator"), or a modulator using a semiconductor electroabsorption effect (hereinafter, "EA modulator"), and the EA modulator, in particular, has become increasingly popular in recent years due to its ability to be integrated with the semiconductor laser, and its good cost benefits.

Oki has a high share of the market for EA modulator drivers [2) 3)] , and we build these drivers using a 0.1 μm gate p-HEMT (see TIPS (left)). Its basic function is to amplify the input voltage amplitude in the 0.3 – 1.0 Vpp range (determined by the output specification of the preceding multiplexer stage), and to output a stable voltage amplitude controlled to a range of 2 – 3 Vpp.

In addition to this, in order to optimize the optical output waveform of the EA modulator, functions for controlling the cross point and the DC offset level, etc. are also required. The circuit is constituted by a three-stage differential amplifier, which is designed to produce an overall circuit gain of at least 20 dB, in order that the input voltage amplitude will be saturated. The 0.1 μm gate p-HEMT is suitable for circuits requiring both of high frequency and high gain of this kind. Fig. 3 is a micro-photograph of the IC. The chip size is 2.3 mm x 1.6 mm.

Fig. 4 shows the optical waveform of EA modulator driven by this IC. The input signal is a pseudo-random bit sequence of 231 –1 at 10 Gb/s. The driver is adjusted so that the cross point of the optical

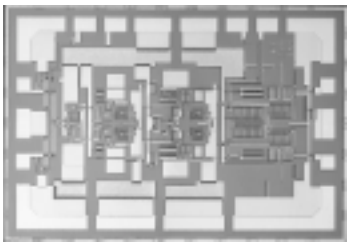

Fig. 3 Photograph of EA driver IC chip

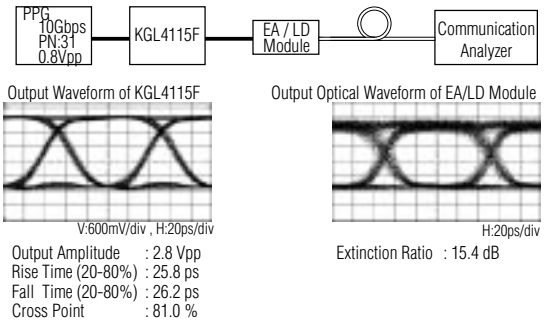

Fig. 4 Operational example of EA modulator driver

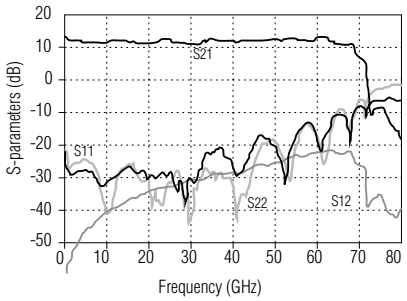

Fig. 5 Small-signal S parameter of driver IC for 40 Gbit/s EA modulator

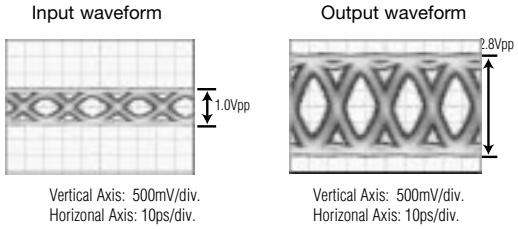

Fig. 6 Input and output waveforms of driver IC for 40 Gb/s EA modulator

output signal is 50%, in which case the output waveform of the driver has a cross point of around 70%. As the diagram shows, excellent high-speed characteristics are obtained, with a waveform rise/fall time of approximately 30 ps, which is sufficiently small with respect to the 10 Gb/s clock cycle (100 ps). Jitter is also small, and the waveform quality is very clean. These are key features of Oki's driver. The extinction ratio observed for the optical is as large as 15.4 dB, and the eye pattern is good. The band width of this IC is 13 GHz or above, which suggests it can be applied to the 12.5 Gb/s system with forward error correction or even the RZ coding system.

(2) 40 Gb/s driver

40 Gb/s optical communications systems (OC-768) are being developed actively all around the world, in order to achieve further an increase in transmission capacity.

Transmission modules used in these systems have almost the same structure as 10 Gb/s system modules, except that a distributed amplifier circuit design is used for the driver IC to gain much wider bandwidth. Fig. 5 shows the RF characteristics of the latest driver IC for a 40 Gb/s EA modulator, which is currently under trial manufacture [4]. This IC provides 11.5 dB gain and a band width as high as 69 GHz.

Fig. 6 shows the output waveform under the condition of the input amplitude of 1.0 Vpp (for pseudo-random bit sequence of $2^{31} - 1$). Even though the 40 Gb/s input signal supplied from a pulse pattern generator used in this experiment is not especially clean, which results in a considerable waveform jitter of the driver output, we still have observed 2.8 Vpp as an output, which may be sufficient for the application.

IC for receiver

(1) Transimpedance amp

This IC amplifies a very small current signal from PD to convert it to a voltage signal. The circuit consists of a three-stage single-ended amp operated by the single power supply of –5V with power consumption of 0.5 W and with transimpedance of 1 kΩ or above [5]. As well as high sensitivity to detect the small input signal, this circuit must also generate a clear output waveform under the large input signal (Optical Over Load). One of the features of this IC is such an internal Auto Gain Control (hereafter, "AGC") circuit to suppress the distortion in the waveform under the over loaded condition. A micro-photograph of the chip is shown in Fig. 7. The chip size is 1.6 mm x 1.3 mm.

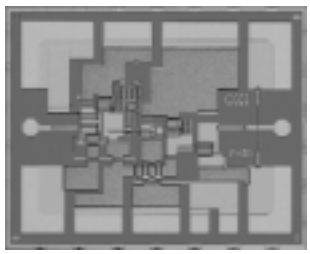

Fig. 7 Photograph of transimpedance amp chip

Fig. 8 is the output waveform of the transimpedance amp corresponding to the optical signal input to a photodiode connected to the IC input. Output waveforms are shown for the respective optical powers of -20 dBm, -5 dBm and 0 dBm in the input signal (pseudo-random bit sequence of $2^{31} - 1$) to the PD. A good eye pattern is obtained even at the lowest input of –20 dBm, and with large amplitude inputs of –5 dBm or above, the AGC function activates automatically to reduce the gain, and hence to suppress waveform distortion.

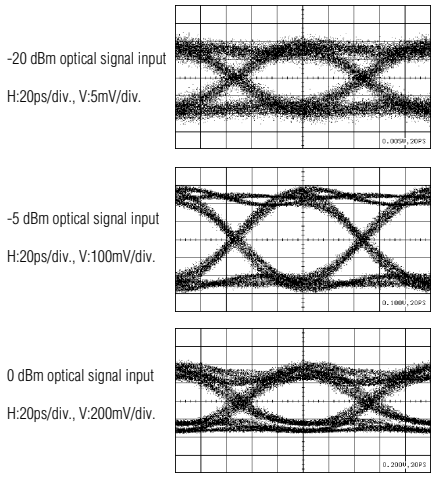

Fig. 8 Output waveform of transimpedance amp

In Fig. 9, we can see the dependence of the measured bit error rate on the input optical power. A BER of 10^{-9} or less is obtained at minimum optical input power of –21.2 dBm and maximum optical input power of +4.3 dBm, which represents a very broad dynamic range (25.5 dB).

(2) Limiting amp

This IC amplifies the small signal from the transimpedance amp so that the output signal has a fixed voltage amplitude, whatever the input amplitude. It is implemented by a Direct Coupled FET Logic inverter (See TIPS (right)) using a 0.2 µm gate GaAs MESFET fabricated by ion implantation technology.[6] Fig. 10 shows a micro-photograph of this chip, which has dimensions of 1.2 mm x 0.9 mm.

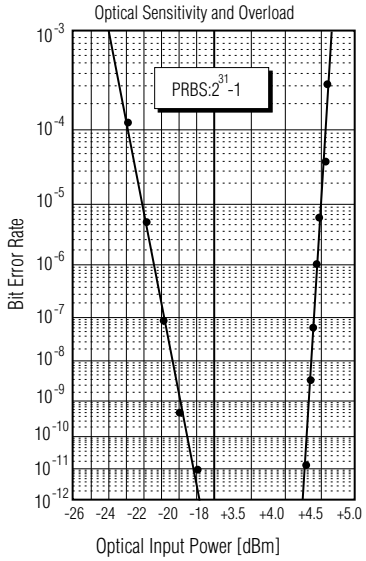

Fig. 9 Dependence of bit error rate on optical input power

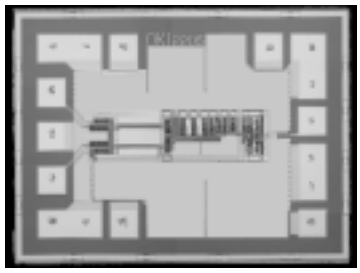

Fig. 10 Photograph of limiting amp chip

One of the features of our limiting amp is its minimal power consumption of 0.25W, which benefits overall power reduc-tion in the reception module. The key performance factor required of this IC is the input sensitivity (the minimum signal level detectable), and Oki's amp has good sensitivity of 10 mVpp.

Conclusion

Here, we have introduced an IC set for an optical transmission module developed using GaAs FET and HEMT. A high performance of such transistors is a key to realize a high performance of the module as a final product. Our GaAs IC for 10 Gb/s transmission system has shown superior strength in performance over our competitors, and has made a big contribution to the expansion of Oki's optical communications components business, riding the US-centred boom in this field since last year. We are currently feeling the effects of a downturn in this market, but actual demand for information communications is still increasing, and we will doubtless see a return to strong growth in the near future. Users are continually requiring inexpensive devices which combine improved performance with excellent reliability and manufacturability. The GaAs IC is one of the high-speed devices which meets all of these needs, and is still competitive with emerging SiGe devices which have made remarkably technological progress. In the future, as well as improving basic device performance and manufacturability, the technological strength of total solutions, which incorporate integration and assembling technology, will be a key factor in beating off rival designs.

References

1) Kimura : "Electronic Materials", p.32, November 2000 (in Japanese)
2) A. Nishino, et. al.: OFC Technical Digest, p.365, 1999
3) Kimura, et. al.: "Electronic Materials", p.xx, November 2000 (in Japanese)
4) Kogawa, et. al.: 2001 IEICE Conference, C-10-17 (in Japanese)
5) H. Ikeda, et. al.: GaAs IC Symposium Technical Digest, 2000
6) H. Yamada, et. al.: Ga As IC Symposium Technical Digest, p.273, 1999
7) T. Ohshima, et.al.: Solid-State Electron. 43, p.1519, 1999

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0.1 µm GaAs p-HEMT device technology

For operating at 10 Gb/s, the transistor used in IC must have a cut-off frequency (ft : max. frequency for amplification) of around 50 – 60 GHz (i.e., 5 – 6 times the bit rate). Fig. 11 shows the GaAs pseudo-morphic HEMT ("p-HEMT") with 0.1 µm gate length used by Oki.7)

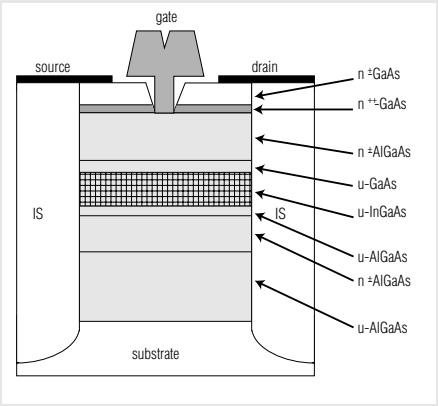

Fig. 11 Cross-sectional structure of 0.1 µm GaAs p-HEMT

Fig. 12 shows a cross-sectional view of the 0.1 µm gate p-HEMT fabricated with this structure, and the frequency characteristics of this transistor. The ft value extrapolated from the current gain is as high as 104 GHz. In order to reduce the gate series resistance, the structure of the gate electrode so-called "mushroom-shaped" is applied, which also results in an excellent noise characteristics. This type of the transistor is particularly suitable for high-frequency analogue circuit.

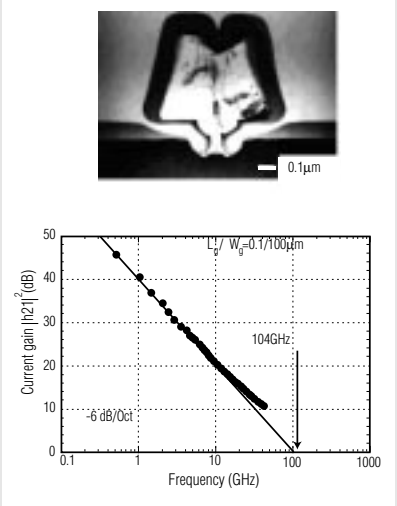

Fig. 12 Cross-sectional SEM photograph of 0.1 µm GaAs pHEMT, and graph of S parameter

0.2 µm gate GaAs MESFET and Direct Coupled FET Logic

Oki uses a 0.2 µm gate GaAs MESFET as the device for its 10 Gb/s digital ICs. A cross section of the device structure is shown in Fig. 13.

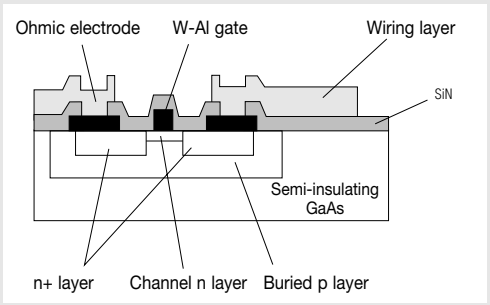

Fig. 13 Cross-sectional structure of 0.2 µm GaAs MESFET

As a configuration for high-speed GaAs digital circuit, either SCFL (Source Coupled FET Logic) or DCFL (Direct Coupled FET Logic), as illustrated in Fig. 14, is possible.

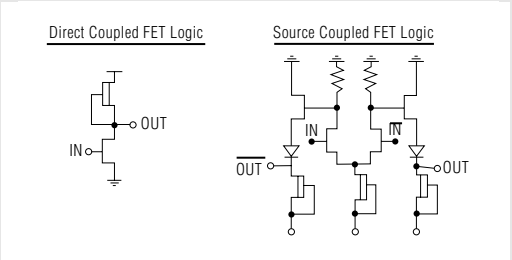

Fig. 14 Circuit composition of Source Coupled FET Logic and Direct Coupled FET Logic

SCFL is based on a differential circuit, and can be implemented only by using a depression-type FET. It has large tolerance margins with respect to the deviation in the performance from transistor to transistor within the IC, so is suitable for high-speed operation. However, because the configuration is not simple it is not suitable for low power consumption designs or large-scale integration. DCFL, on the other hand, uses a simple circuit structure operated on a single ended signal, and since it is able to operate at a power voltage of 2V or less, it is suitable for low-power ICs. With a switching speed of 10.4 ps (at 2V drain voltage), satisfactory high-speed characteristics for 10 Gb/s operation are confirmed. Moreover, the standard deviation of the delay time in the wafer is as small as 0.28 ps (2.7%), which means the device has the sufficiently uniform characteristics required in designing large-scale digital ICs.

Since the channel in the GaAs MESFET is formed by ion implantation technology, it is possible to fabricate FET with different threshold values on the same chip, which enables easy application to DCFL circuits like that described above.