Forming sub-100 nm contact holes

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Progress in microfabrication technology has played a fundamental role in achieving higher density and capacity in semiconductor devices. In photolithography, currently the main technology used in microfabrication, it has been possible to shrink pattern sizes by around 70% over 3 years, by moving to shorter optical wavelengths for exposure, and improving resolution in both exposure optical systems and photoresist materials. At present, mass production of 150 nm patterns has become possible through a KrF photolithographic process using a KrF excimer laser light source operating at an optical wavelength of 248 nm.

Recently, however, there have been demands to advance miniaturization schedules ahead of current development trends. Yet the enormous investment of both money and labour required to develop next-generation technology (for example, 193 nm-optical wavelength ArF excimer laser lithography) is a major impediment to achieving early mass production. One way around this is the adoption of shrinkage technology, which achieves next-generation level pattern sizes by combining various additional processes with conventional photolithography, and this technology is an important focus of research at the present time.

The two main shrinkage technologies proposed to date for use in photolithography involve either generating a thermal flow in the photoresist by high-temperature heat treatment, or forming a mixed layer of resist and another material. This paper reports sub-100 nm contact hole formation technology which combines thermal flow in the resist with a KrF photolithographic process (below, “Thermal Flow Process” is abbreviated as “TF Process”).

Characteristics of thermal flow process

Conventionally, thermal flow has not been seen as a desirable method for forming resist patterns, due to deterioration of the pattern shape. However, it has confirmed that, in KrF photolithography, the contact hole dimensions can be shrunk accurately, if the resist thickness, initial pattern dimensions, and thermal treatment (bake) temperature and other conditions are set correctly. As for the alternative shrinkage technology, mixing layer formation, proposed methods include the resin overcoat technique[1)] developed by Oki for I-line (365 nm wavelength) lithography, and a RELACS method, etc. for KrF lithography.[2)]

Fig. 1 shows the sequences of the respective processes. In either case, the resist coating, exposure and development steps are carried out in exactly the same way as a standard process. In the TF process, this is followed by a single shrink bake processing step, and the whole sequence can be set up in a current coater / developer apparatus.

The mixing layer formation process, on the other hand, involves additional steps for coating the mixed material, mixing bake, and rinsing (to eliminate unwanted parts with special rinse solution), once the standard pattern forming steps have been completed.

From the above, TF process appears to be the easiest method to introduce, due to the simplicity of the process and its compatibility with existing mass-production facilities, and we therefore studied TF process in closer detail.

Basic characteristics of thermal flow process (1)

Fig. 2 shows a pattern before and after shrinking. Fig. 2(a) shows contact holes of 280 nm diameter, formed by standard processing of an acetal type KrF resist A (hereinafter, called KrF resist A) coated to a thickness of 1.06 µm. Fig. 2(b) shows the same resist pattern after baking at 137°C for 60 seconds. These settings allow formation of a pattern of contact holes approximately 100 nm in size.

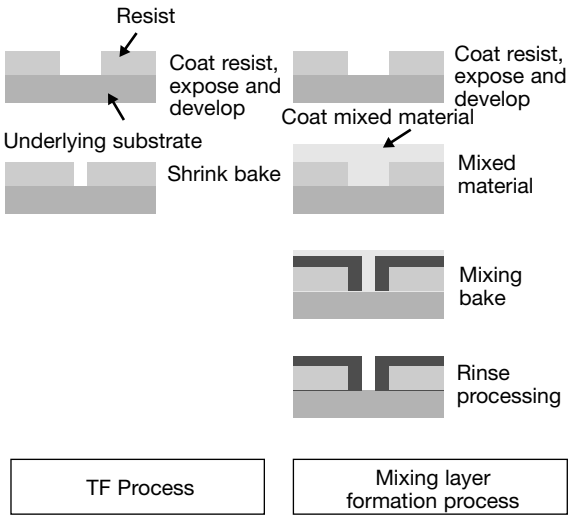
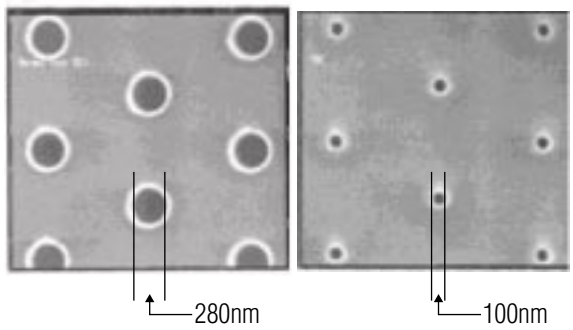


Fig. 1 Process flows of TF and mixing layer formation processes



(a) Before shrinking (b) After shrinking

Fig. 2 Pattern size before and after shrinking

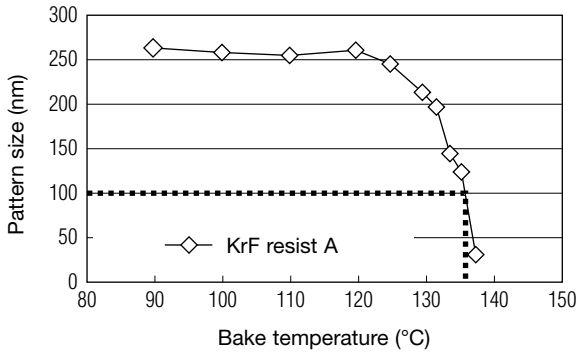
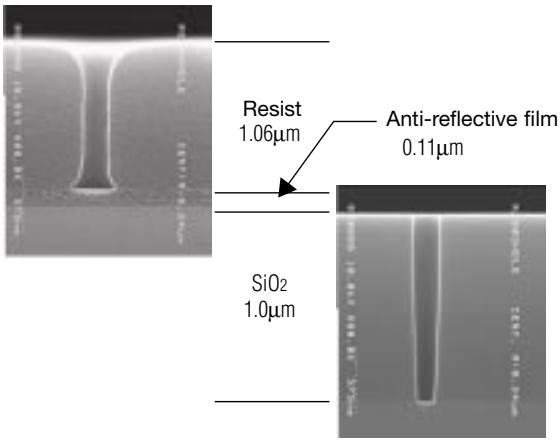


Fig. 3 Relationship between pattern size and bake temperature

In TF process, the dimensions after shrinking are strongly influenced by the bake temperature. Fig. 3 illustrates this relationship between shrink bake temperature and pattern size. The KrF resist A shows virtually no change in dimensions when the bake temperature is in the range 90 – 120°C. However, shrinkage starts abruptly in the region of 125°C, and by 137°C, the pattern dimension is reduced to the 100 nm level. Around this temperature, the change in size is approximately 30 nm per 1°C. In this way, precise temperature control is required to obtain the desired amount of shrinkage.

Fig. 4(a) shows a cross section of a resist pattern after shrinking. This pattern was fabricated by forming an anti-reflective film (0.11 µm thick) onto the processed film (SiO_2 1.0 µm thick), coating this with KrF resist A (1.06 µm thick), and then shrinking the pattern from 280 nm to 100 nm. A thermal flow was created by heating the resist above the glass transition temperature, and rounding or erosion occurred in the top and bottom sections as a result of the surrounding resist flowing into the contact holes, but in the central region, vertical regions 100 nm in diameter and 0.7 µm high were formed.

Fig. 4(b) shows the results of etching the underlying antireflection film and the SiO_2 film using this resist pattern as a mask. In the TF process described above, a pattern of contact holes with an internal diameter of 100 nm or less was formed in a 1.0 µm thick SiO_2 film.



(b) After shrinking (b) after etching

Fig. 4 Pattern cross-sections

Table 1 Comparison with rival companies' processes

	Oki TF conditions	Rival conditions
Resist film thickness	1.06µm	0.57µm
Exposure technology	NA=0.50 Normal exposure Binary mask	NA=0.60 Phase shift mask
Initial dimensions	280nm	180nm
Dimensions after shrinking	80nm	120nm

Other device manufacturers, particularly Korean suppliers, have been investigating processes which use this thermal flow of the resist.[3) 4)] Table 1 shows a comparison between typical process settings. Whereas rival companies have based their approach of the use of cutting-edge techniques, such as phase shift masking, to reduce the initial pattern size, thereby also reducing the amount of shrinkage, Oki's TF process is characterized by its use of conventional exposure technology and the very large shrinkage rates (29%) achieved in reducing a 280 nm pattern to 80 nm.

Basic characteristics of thermal flow process (2)

An actual device combines contact hole patterns of various sizes and layouts. There are two issues to be dealt with in TF process, if the various pattern dimensions required are to be achieved : namely, pattern pitch dependence and pattern size dependence.

Fig. 5 shows how the shrink dimensions are dependent on the pattern pitch. The graph shows the change in dimensions for a range of pitches from 0.44 to 3.0 µm, at a uniform contact hole mask size of 280 nm. From a pitch of 3.0 µm to around 1.0 µm, the post-shrink dimensions are virtually the same, but from 1.0 µm onwards, the amount of shrinkage gradually starts to decline, and below 0.6 µm it falls abruptly. This is thought to be a result of the fact that the close proximity of the patterns causes mutual interference between the

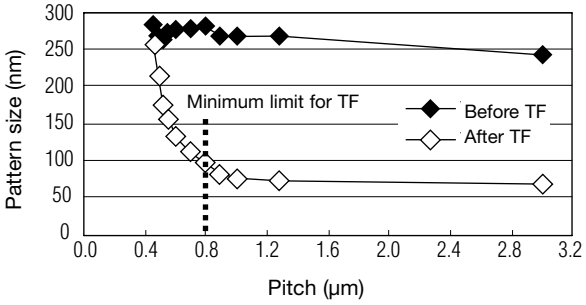


Fig. 5 Relationship between shrink dimensions and pattern pitch

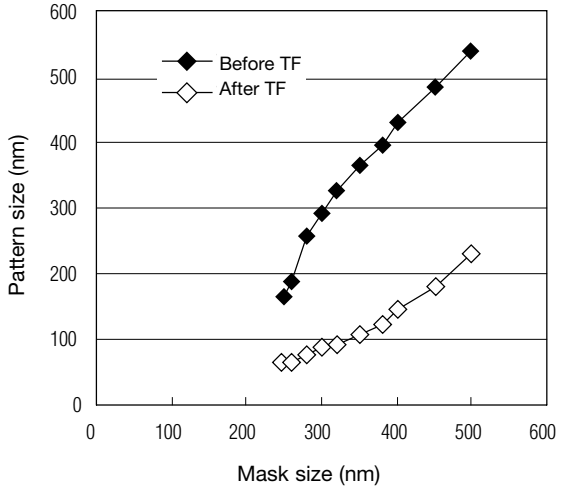


Fig. 6 Relationship between shrink dimensions and pattern size

patterns due to surface tension, which effectively cancels out the thermal flow shrinkage effect. On the other hand, if the patterns are separated at a pitch of 1.0 μm or above, then the TF process can be viewed in isolation, and a virtually uniform rate of shrinkage can be achieved.

Fig. 6 illustrates how the shrink dimensions are dependent on the pattern size. Here, it is important to note the shallow gradient of the graph of post-shrink size, compared to the pre-shrink graph. This is particularly notable at a pre-shrink dimension of 300 nm or less : shrinking patterns of 200 – 300 nm results in post-shrink sizes of 70 – 100 nm, a large reduction in the dimensional range.

Using TF process in devices : evaluation

In contact hole processing for a DRAM, contact holes with sub-100 nm final dimensions are used. These are very small holes which clearly exceed the 200 nm practical limit of contact holes formed by current KrF lithography. Therefore, techniques for shrinking the contact holes by lamination of inorganic film, or the like, have been adopted. However, these approaches require many complicated processes and give rise to various problems, such as increases in TAT, defect density, and equipment load. We investigated the possible application of thermal flow technology as a way of simplifying this process.

The main problem in evaluating this application to a device was that of pattern size uniformity in the wafer area. When a TF process using KrF resist A was applied to an 8-inch wafer, the dimensional range in the wafer area was relatively large, at approximately 90 nm (60 – 150 nm), with respect to the target size of 80 nm. This led us to look carefully at different resist materials, bake unit structures, baking methods, and so on, research which revealed the benefits of changing to an acetal type KrF resist B having a different composition ratio. This resist reduced the wafer area variation to some 40 nm, about one half of the figure achieved with KrF resist A.

Fig. 7 illustrates size fluctuations between different wafers processed in a continuous system. Flow 1 was based on a standard processing method, which showed large size variations in the first 6 wafers processed. This is due to slow temperature response in the shrink baking step, which gives rise to unstable temperature conditions during processing. Flow 2 uses timing adjustment in the shrink bake process, to ensure that the wafer processing interval is uniform. This modification reduced the variation between wafers to some 8 nm.

Table 2 shows dimensional settings for a cell section and peripheral circuit section in the case of a normal process and a TF process. These values have been derived from the graphs of shrink rate against pattern pitch and pattern size shown in Fig. 5 and Fig. 6, but they were reproduced with good accuracy in device processing. This proved that highly accurate size corrections can be achieved, by means of a database created from a standard evaluation pattern.

Lastly, in Fig. 8, we can see the dimensional stability of the 64 wafers used to evaluate the TF process. A stable size variation of 3σ = 23 nm was obtained. By constructing a suitable framework to ensure resist material stability, equipment stability, and lot dimension management, etc., it is possible to maintain satisfactory, stable conditions.

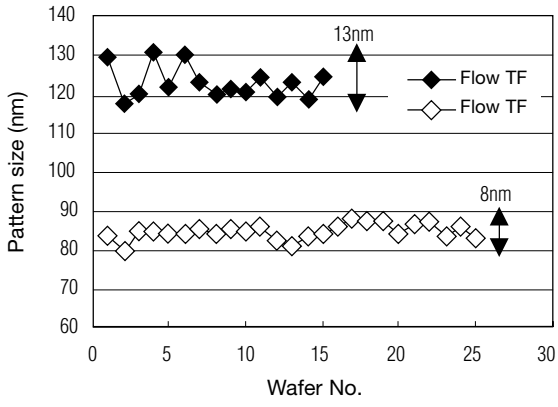


Fig. 7 Dimensional stability in continuous processing

Table 2 Dimensional balance of cell section and peripheral circuit section

	Normal process		TF process	
	Mask (nm)	Finished (nm)	Mask (nm)	Finished (nm)
Cell	280	100	280	100
Peripheral	320	130	460	130

Conclusion

By using KrF lithography and thermal flow process of the resist layer, we have been able to form sub-100 nm contact holes. By means of simple process settings, wide-ranging shrinkage from 280 nm to 80 nm can be achieved, meaning that existing coaters, developers and exposure equipment can continue to be used.

Moreover, by clarifying the pattern pitch dependence and pattern size dependence which are intrinsic characteristics of TF process, we have been able to establish correction procedures to use when applying TF process to devices.

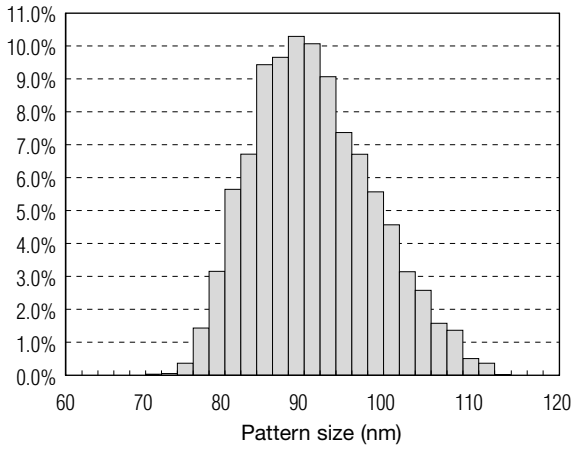


Fig. 8 Long-term dimensional stability

Our future research will look at all aspects of shrinkage technology, from resist materials, bake unit structures, to baking methods, and beyond, in order to achieve greater dimensional uniformity, improve the pattern pitch and pattern size dependence, and enhance stability.

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