

# Multi-chip package with built-in W-CSP enables development of system LSI for high-density devices

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The multi-chip package (or MCP) uses packaging technology to install several chips in a single package. The MCP is a type of System in a Package (SiP), which is one of the methods used to ensure system LSI functionality. The other method is system on chip (SoC), but SiP has the advantage of comparatively lower development times and costs. This has led to a rapid expansion in demand, focussed principally on mobile, small-scale devices with short product cycles. The required functions can be achieved by combinations of existing chips, or by mixing existing chips with simplified chips which provide custom functions. Either way, this enables time and cost savings compared to a new chip developed from scratch. Furthermore, housing a number of chips in a layered structure in the same package means that high-density installation can be achieved.

We have developed an MCP with built-in Wafer-level Chip Size Package (W-CSP) with the aim of providing low-cost layering at uniform chip size for the small, portable device market. The advantages and development results of our MCP with built-in W-CSP are described in this paper.

## Problems of wire-bonded MCPs

Wire bonding (hereinafter, WB) is the standard method used for current MCPs. Fig. 1 shows cross sections of the structure of a WB type MCP. A first chip is installed on the package substrate, and a



Fig. 1 Sectional structure of wire-bonded MCP

second chip is then mounted on the first chip. Both chips and the substrate terminals are connected by wires. A key feature of WB is low overall costs, including substrate and resin moulding costs.

However, WB does present two problems:

- (1) It does not permit layering of same-size chips;
- (2) Layering is not possible if the first chip has a centre pad.

The first problem arises because a WB region must be ensured on the first chip. Therefore, chip size restrictions apply, if both the upper and lower chip are of the same size, or if the second chip is bigger, etc. For example, when a logic LSI is combined with a flash memory, in some cases, the difference in shrink speed during wafer processing means that any disparity in chip size will be eliminated by chip shrinkage.

The second restriction applies to devices, such as a DRAM, which have a pad mounted in the centre of the chip. In such cases, laminating a second chip will obstruct WB connection to the first chip.

	FC method at chip level		Built-in W-CSP
	Heated pressure bonding	Metallic bonding	
Diagrams			
Overall	X	X	○
First chip	○ Normal (same as WB)	○ Normal (same as WB)	△ Rewiring (W-CSP)
Substrate	X High-density wiring substrate	X High-density wiring substrate	○ Two-layer rigid substrate
Underfill	X ACF, NCP, etc.	X Liquid resin	○ Transfer resin
First chip mounting method	X Independent mount FC bonder	X Independent mount FC bonder	○ Universal reflow (SMT technology)

Fig. 2 Characteristics of various flip chip-type MCPs

### Comparative testing of flip-chip type MCPs

The restrictions on chip size and pad position described above can be resolved by using a flip-chip (hereinafter, FC) type MCP. With FC technology, a first chip formed with a bump on the pad is pasted directly onto the substrate terminals to form an electrical connection with the terminals. A second chip is then mounted on this chip, and connected electrically to the substrate terminals by wire bonding. Broadly speaking, there are three types of FC method, as illustrated in Fig. 2, depending on the type of first chip and how it is pasted onto the substrate.

The first FC method is a heated pressure bonding process, in which stud bumps formed on the pad of the first chip are heat and pressure bonded with the substrate electrodes by means of an adhesive inserted between the bumps and electrodes. The adhesive used may be an anisotropic conductive film (ACF) containing conductive granules, an anisotropic conductive paste (ACP), a non-conductive film (NCF) which does not contain conductive particles, or a non-conductive paste (NCP), etc.

The second method is a metallic bonding process. Here, stud bumps formed on the pad of the first chip are bonded metallically with the substrate electrodes by printed or plated metal to achieve electrical connection. Ag-Sn, or the like, is used for the substrate electrodes. In addition, a liquid resin is used as a spacer between the first chip and the substrate.

Both the first and second methods require substrate with high-density wiring. They also use separate mounting systems employing flip-chip bonder equipment.

On the other hand, the MCP incorporating W-CSP recently developed by Oki is based on an FC method which uses W-CSP as the first chip, and achieves functional operation by metallic bonding solder bumps on the W-CSP to the substrate electrodes.

The first chip used is reconfigured into an array by rewiring the peripheral layout pads used in the WB method. Therefore, by increasing the pitch between the pads, a general rigid substrate with two-layer dual-face wiring can be used, instead of requiring a high-density wiring substrate. The gap between the first chip and the substrate is filled with a universal moulding by a standard transfer method. An alternative method comprises two separate steps: one to fill liquid resin into the gap, and one to seal the mould of the second chip and wires, but it is also possible to use universal moulding by optimizing the moulding conditions. The W-CSP can also use a standard universal reflow process (SMT : Surface Mount Technology) for package mounting.

Fig. 3 shows cost comparisons for MCPs based on the FC methods described above. The MCP with built-in W-CSP can be built for 70% of the overall cost of the heated pressure bonding method, which is depicted as 100% in the graph.

In addition to these benefits, it is also possible to reduce the pin number on the first chip, by strengthening the power supply and ground wires

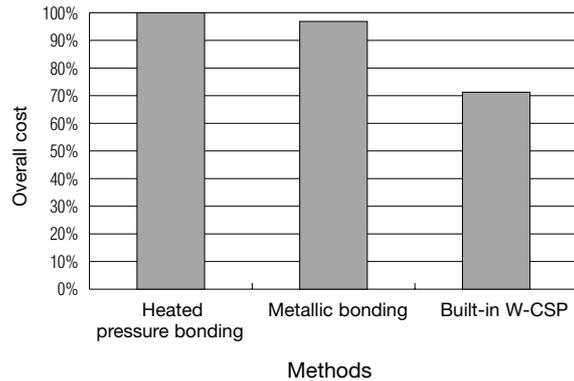


Fig. 3 Cost comparison of FC-type MCPs

through rewiring inside the W-CSP. This rewiring of the W-CSP also allows designers to add extra functions.

The major advantage of incorporating a built-in W-CSP is the high reliability that this affords. W-CSPs adopt a stress-relieving structure in order to guarantee the reliability of their internal connections, and they can be expected to create more reliable junctions than other types of flip chip. Improved humidity resistance can also be anticipated, since the chip surface is sealed with high-quality resin.

For the above reasons, a built-in W-CSP solution was adopted to provide same size chip compatibility in a MCP.

### Development results of MCP incorporating W-CSP

Fig. 4 shows the processing flow of an MCP incorporating W-CSP. Three of the key aspects borne in mind during the development of this package are discussed separately below.

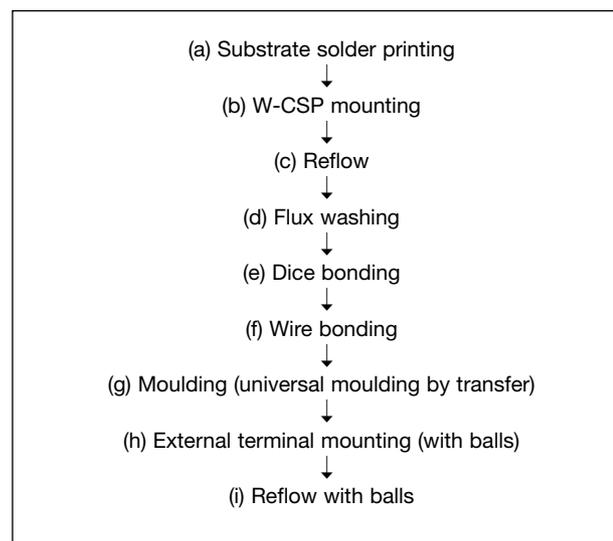
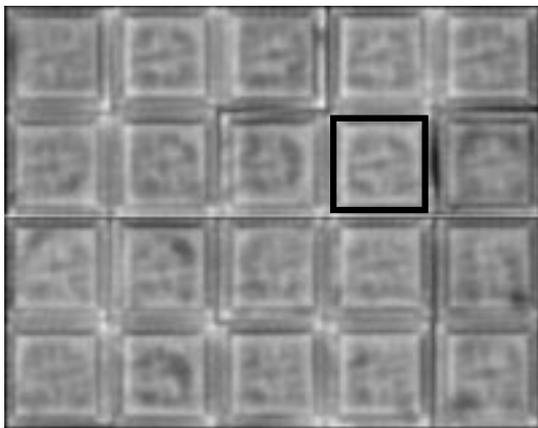


Fig. 4 Processing flow for MCP incorporating W-CSP

### (1) Use of lead-free solder

Due to environmental concerns, we used lead-free solder for the W-CSP solder bumps, and the external solder balls for package mounting. This type of solder has a higher melting point than eutectic solder, which means that the reflow step (c) and ball installation reflow (i) can be carried out at high temperatures.

In a reflow tolerance evaluation modelled on mounting carried out after packaging, the MCP achieved level 2 of the JEDEC (Joint Electron Device Engineering Council) standards (storage limit one year at 303K and 60% RH after dry pack sealing) when subjected to hot reflow for lead-free solders (max. 533K). Flaking and cracking in the MCP after reflow was evaluated using a transparent type scan acoustic tomograph (abbreviated here to "transparent SAT"). This type of analysis is generally performed with a reflective type SAT, but since the MCP incorporating W-CSP has a multi-layer vertical structure with a plurality of interfaces, it requires a transparent SAT. Fig. 5 is a transparent SAT image of the package interior after reflow. The photograph shows the result for a group of 20 packages – each square frame in the picture is one package. The image shows no indications of flaking or cracking.



ig. 5 Transparent SAT results after reflow

### (2) Wire bonding

In an MCP with W-CSP, the second chip is assembled by wire bonding (WB). Therefore, since solder terminals are already present when the package is heated, the WB temperature must be kept below the melting point of the solder. For this reason, the wire bonder is set to high-frequency (120 kHz) ultrasonic operation and the WB conditions are optimized, so that stable wire bonding can be achieved at low temperature (413K on chip). As shown by the structural diagram of the W-CSP in Fig. 2, the results are no different to examples where the second chip is bigger than the W-CSP. If the W-CSP is in a floated state, rather than being located beneath the metal ball junctions of the second chip, the transmission efficiency of the ultrasonic waves used

in wire bonding will decline, but bonding strength equivalent to that of existing packages can still be ensured.

Fig. 6 shows WB results for a case where the second chip is smaller than the W-CSP. By optimizing the WB conditions, shorting of the wires at the edges of the W-CSP can be avoided.

All of this means that wire bonding is compatible with second chips which are both smaller or larger than the W-CSP.

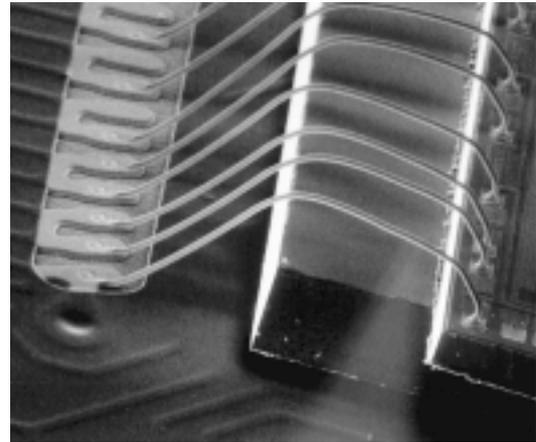


Fig. 6 WB results for second chip (wires extending beyond W-CSP)

### (3) Interval between W-CSP and substrate

To reduce W-CSP thickness, it is necessary to narrow the gap between the W-CSP and the substrate. The key to this is careful control of the size of the CSP-to-substrate interval, allied with flux washing (d) and moulding (g) of the narrow interval.

The interval can be controlled by optimizing the amount of solder used in substrate solder printing (a). During the reflow heating (c), the solder melts and if there is too little solder due to the weight of the W-CSP, then the gap cannot be guaranteed, whereas if there is too much solder, then bridging will occur. Therefore, conditions are optimized.

During reflow (c), flux is used between the substrate and the W-CSP. Therefore, in the flux washing process (d), the flow of washing liquid is controlled so that it enters inside the gap between the W-CSP and the substrate.

Also, in order to guarantee reliable connections at the internal terminals, resin is filled into the gap between the W-CSP and substrate. As stated previously, in the alternative FC method, liquid resin is inserted between the first chip and the substrate. By creating a vacuum inside the moulding die, the transfer moulding seal for the MCP incorporating W-CSP can be completed using standard resin in a conventional assembly line, and optimum conditions can be set to avoid any occurrence of voids or wire melting. Without a vacuum in the moulding die, parts of the gap between the first chip and the substrate

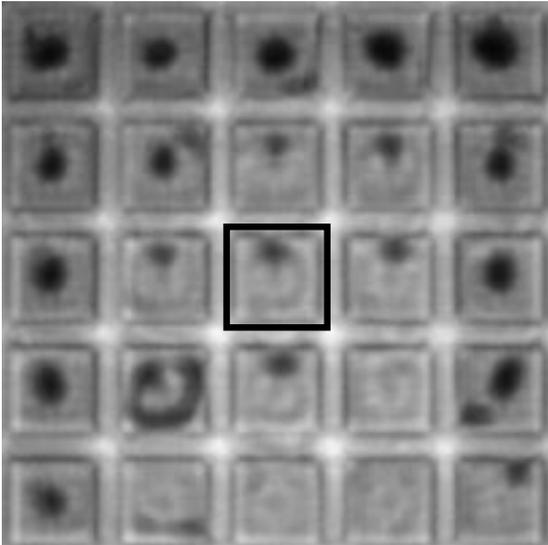


Fig. 7 Internal void observation results  
25 packages (one package per frame)  
Black regions : internal voids

may remain unfilled. Fig. 7 shows observation results for these internal voids, as viewed by a transparent SAT. The photograph covers 25 packages, each square frame being one package. The black regions indicate the voids.

### Conclusion

Oki Electric has developed an MCP incorporating W-CSP which permits layering of same size chips and the use of lead-free solder.

This has increased the range of chips which can be used in Multi Chip Packages, and opens the way for development of system LSI products which are compatible with a wide variety of applications.

Oki is already designing system MCPs of this kind and is excellently placed to actively propose new products and bring them swiftly to market, through careful system selection.

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## TIPS

### Basic Terminology

#### System in a Package (SiP)

An SiP provides a system in a single package by integrating all required functions the same package.

For example, CPU, memory and logic functions might all be incorporated into a single package.

#### System on a Chip (SoC)

A system is provided in a single chip, by integrating all the functions into the same chip.

#### W-CSP : Wafer-level Chip Size Package

This is a new concept in packaging : all assembly steps are completed at the wafer stage. On the outside, the package looks like an FBGA (Fine Pitch Ball Grid Array), with terminals arranged in a lattice on the rear face of the package.

At Oki Electric, we use metal plate films to rewire and space out LSI chip bonding pads, and we apply solder balls (or solder coatings) to chip terminals.

The main advantages of Oki's W-CSP are:

- (1) By using rewiring to increase the ball pitch, we can reduce the wiring density on the mother board, which reduces costs, as well as providing easy board mounting for the customer.
- (2) Metal tower posts (metallic layers) are provided under the solder balls or solder coats to ease stress, and to improve the reliability of the solder connections.
- (3) The chip surface is sealed with a high-quality epoxy resin, which protects the chip surface from flux during mounting and avoids the need for special processing in flux washing.