Next-generation low-power consumption SOI devices

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Low-power, high-performance LSIs are a widely anticipated technology for next-generation personal and mobile communications products. In the past, the typical low-power devices have been bulk silicon CMOS devices (bulk CMOS), but LSI power consumption has risen with the new levels of speed and integration brought by increasing miniaturization, and we are currently looking towards new power reduction techniques which will cover both design procedures and element structure. In these circumstances, a fully depleted SOI CMOS (FDSOI-CMOS) is expected as one of the next generation of low-power-consumption devices.[1) 2)]

Here at Oki, we have introduced the world's first commercial FDSOI LSI.[3)] The surface area of the LSI section is reduced by 50%, and current consumption, by some 75%, compared to a conventional LSI. By exploiting the particular characteristics of FDSOI CMOS devices, we have been able to achieve LSI products which have special features compared to bulk CMOS, whilst making use of existing design assets.

This essay examines the low-power-consumption characteristics and performance of FDSOI CMOS devices, using scaling models based on conventional bulk CMOS, and discusses the future possibilities of FDSOI technology.

Bulk CMOS scaling models

Bulk CMOS devices were launched and evolved as low-power-consumption devices. However, with the increases in LSI operating frequency which have accompanied scaling-based increases in element performance, as well as the rise in the capacitance value to be charged and discharged per unit area, a result of reduced oxide film thicknesses and increased junction capacitance in the diffusion layer, LSI power consumption has risen as scaling has progressed. More detailed information is given in the Appendix, but Table 1 shows calculated values for performance, integration level and power consumption in respective device generations, based on bulk CMOS scaling rules. Supposing the case of a 10 mm square LSI chip, whilst the power supply voltage is declining, the power consumption is increasing by about 10% with each generation advanced, and at thicknesses of 0.18 μm and below, a 100 mm^2 chip would require over 100 W of power.

Conditions for low-power devices

Two of the key conditions required in the low-power-consumption devices to replace bulk CMOS are good affinity with bulk CMOS LSI design, and easy incorporation

Table 1 Performance comparison for bulk CMOS LSIs of different generations

Gate length (μm)	0.35	0.25	0.18	0.15	0.13	0.1
Gate width (μm)	2.751	1.965	1.4148	1.179	1.0218	0.786
1M layout pitch (μm)	0.917	0.655	0.4716	0.393	0.3406	0.262
Wiring width (μm)	0.4585	0.3275	0.2358	0.1965	0.1703	0.131
Gate number per 100 mm^2	2.83E+06	5.55E+06	1.07E+07	1.54E+07	2.05E+07	3.47E+07
Power supply voltage (V)	3.5	2.5	1.8	1.5	1.3	1
Threshold voltage (V)	0.875	0.625	0.45	0.375	0.325	0.25
Oxide film thickness (A)	77.8	55.6	40	33.3	28.9	22.2
Oxide film capacitance (F/m^2)	4.44E-03	6.22E-03	8.63E-03	1.04E-02	1.20E-02	1.55E-02
Effective drift rate (cm^2/Vsec)	2.65E+02	2.42E+02	2.26E+02	2.19E+02	2.14E+02	2.08E+02
Tr on current (A/m)	447	483	531	564	593	655
Tr input capacitance (F)	4.27E-15	3.05E-15	2.20E-15	1.83E-15	1.59E-15	1.22E-15
On resistance (Ω)	2.13E+03	1.97E+03	1.80E+03	1.69E+03	1.61E+03	1.46E+03
Gate pitch (μm)	1.21E+01	6.71E+00	3.99E+00	2.82E+00	2.47E+00	1.94E+00
Average wiring length (μm)	63.95	36.66	22.48	16.14	14.34	11.54
Wiring capacitance (F/m)	1.82E-10	2.19E-10	2.74E-10	3.13E-10	3.48E-10	4.27E-10
Wiring resistivity (Ω/cm)	1.61E+03	2.26E+03	3.14E+03	3.77E+03	4.35E+03	5.65E+03
Gate input capacitance (F)	1.15E-13	8.24E-14	5.93E-14	4.95E-14	4.29E-14	3.30E-14
Output resistance (Ω)	710.9	658.2	598.6	563.7	536.1	486
Drain junction capacitance (F)	1.07E-14	7.46E-15	5.29E-15	4.38E-15	3.78E-15	2.89E-15
Average gate delay (psec)	272.1	179.3	118.1	92.5	77.3	55.5
OFF LEAK current (A/m)	6.72E-17	3.00E-14	2.15E-12	1.34E-11	4.56E-11	2.84E-10
Standby power (W)	9.32E-10	4.17E-07	2.99E-05	1.87E-04	6.32E-04	3.95E-03
Max. operating frequency (MHz)	147	223.1	338.8	432.5	517.8	721
Power consumption (W)	88.24	95.66	104.6	111.28	115.46	123.68

of power saving measures into circuitry and architecture.

Development of large-scale LSIs means having to develop high-function LSIs in a short timeframe. In bulk CMOS, it has been sought to improve design productivity by introducing automated design alongside scaling techniques. As conventional scaling procedures demonstrate, the order of priority in LSI development has been high functionality, first, followed by high speed, and then low power consumption, so it has never been possible to reduce power consumption by trading off functionality or speed. This means that new devices must maintain good affinity with the existing bulk CMOS LSI design environment and design assets.

Achieving low power consumption in LSIs also requires incorporation of appropriate measures in each of the respective layers : device, circuit and architecture. Of these, the device influences circuit design and architecture design, so new devices must be chosen carefully to avoid reducing the power saving options available in circuit and system design. Low-power devices require low capacitance values for charging/discharging and elements which give fast operation at low voltages. More details can be found in the Appendix.

Fully depleted CMOS (FDSOI-CMOS) devices

FDSOI-CMOS devices are eagerly awaited as one of the next generation of low-power devices, for the following main reasons:

(1) they have low parasitic capacitance;
(2) threshold values can be set lower than in bulk devices;
(3) the leakage current at idle shows little temperature dependence;
(4) they have good design affinity with bulk CMOS;
(5) the substrate bias effect is low.

These merits are discussed separately below.

Firstly, in a bulk MOS, the parasitic capacitance includes junction capacitance (Appendix : Equation 16), as well as the gate capacitance. In order to suppress short channel effects with increased miniaturization, the impurity concentration under the junction is raised, and this gives rise to increased junction capacitance. An FDSOI-MOS, on the other hand, is formed on a buried oxide film, which means that the surface component of the junction capacitance can be ignored and a junction capacitance some 1/10th that of a bulk MOS can be achieved. By reducing the capacitance subjected to charging and discharging, low power consumption can be achieved alongside high functionality.

One of the main features of FDSOI-MOS devices is their sharp sub-threshold characteristics. This occurs because the elements are formed on a buried oxide film, and therefore the FDSOI-MOS substrate coefficient is 1.05 – 1.1, accounting for the capacitance of the buried oxide film (Appendix : Equation 17), and the S factor value is 60 – 65, which is low compared to 80 – 95 in a bulk MOS. Therefore, at the same idle leakage current, a lower threshold voltage can be set in an FDSOI MOS than in a bulk device. This makes it possible to lower the supply voltage and achieve power reductions, whilst maintaining the same performance as a bulk CMOS. As regards the temperature dependence of the idle leak current, this varies greatly

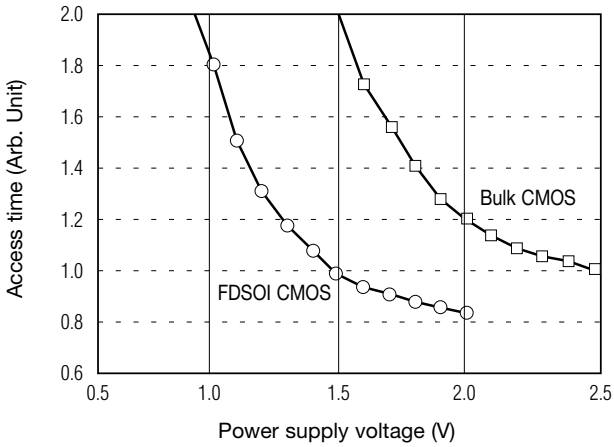

Fig. 1 Comparison of processor core performance

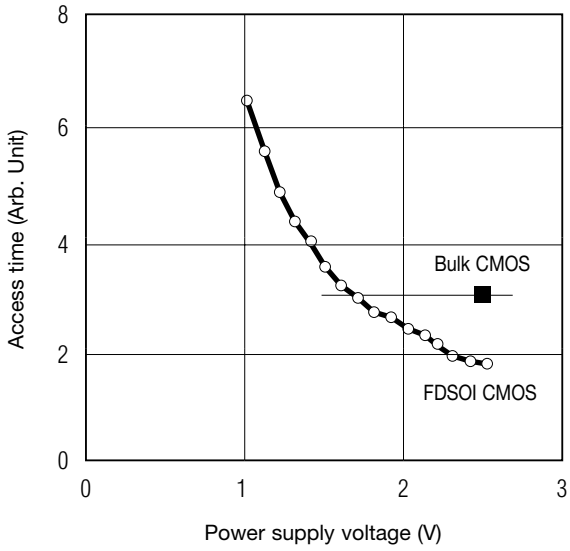

Fig. 2 Comparison of SRAM core performance

between bulk MOS and FDSOI MOS devices, due to their different structures. In a bulk MOS, the leakage current originates from a reverse current in the diode between the drain and substrate, which is proportional to the square of the true carrier density (ni^2). However, in the case of SOI, since the drain is located on the buried oxide film, the leak current depends chiefly on the thermal excitation current, and this temperature dependence is directly proportional to the true carrier density (ni).[4] Therefore, comparing the current at standby on the high-temperature side of the guaranteed operating conditions (85°C), we can see that the FDSOI-MOS is reduced to a standby current some three factors of 10 below that of a bulk MOS.

The FDSOI has high affinity with bulk CMOS devices, and is able to incorporate directly the circuit layout patterns created for existing bulk CMOS. Figs. 1 and 2 shows the results of testing and evaluation using patterns designed for previous bulk CMOS devices. Fig. 1 shows the evaluation results for the performance and power supply voltage of a processor core, and Fig. 2 shows the

corresponding results for an SRAM core. This testing based on bulk CMOS circuit layout pattern confirmed that without any pattern modifications, from 1.5 to 2 times the performance is obtained at the same voltage, whilst power consumption for the same performance is cut by one third, since it is directly proportional to the square of the power voltage. By converting existing elements to FDSOI devices, by making use of existing design assets, we have been able to improve both performance and power consumption. Moreover, further advantages have been gained by adopting layout and circuit models which are most suitable to FDSOI. Since FDSOI devices do not require the substrate terminals needed in bulk CMOS, the chip footprint can be reduced by some 30%. In the past, pipelining has been suggested as a low-power-consumption architecture, and it has been reported that power consumption can be cut by 60% at the same performance, through an approx. 30% increase in the circuit surface area.[5] Using FDSOI technology, the 30% reduction in footprint cancels out the increased area caused by pipelining, and this means that reduced power consumption can be achieved without increasing the surface area of existing bulk CMOS devices.

The fact that FDSOI technology involves building on top of the buried oxide film also gives rise to its characteristically low substrate bias effects. Therefore, in a (vertically integrated) circuit with MOS devices connected in series, there is no downgrading of performance due to increased threshold values caused by substrate bias, and this represents a major performance improvement over bulk CMOS products. Fig. 3 shows an evaluation of the relationship between power supply voltage and delay time in a 4NAND delay circuit. In the FDSOI devices, the absence of substrate bias effects and the low junction capacitance mean that the same performance as a bulk device can be achieved at one half of the voltage. As a result, significant gains in performance and power consumption can be obtained if FDSOI technology is used

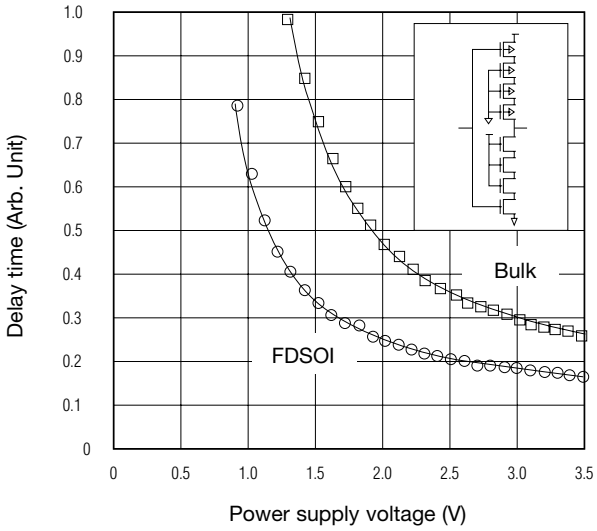

Fig. 3 Comparison of performance in 4NAND vertically integrated transistor

in a pass transistor logic circuit model, for instance.[6] By changing from the NOR logic used in memory LSIs to NAND-based architecture using vertically integrated MOS devices, which could not be adopted in previous bulk CMOS devices due to the associated performance losses, major reductions in power consumption can be achieved whilst preserving performance at the level of bulk CMOS devices based on NOR logic.

Further steps to power reduction using FDSOI

We also calculated the effects of FDSOI parasitic capacitance on the bulk CMOS power consumption and performance model, and these results are shown in Fig. 4.

Assuming that a 10 mm square bulk CMOS LSI was

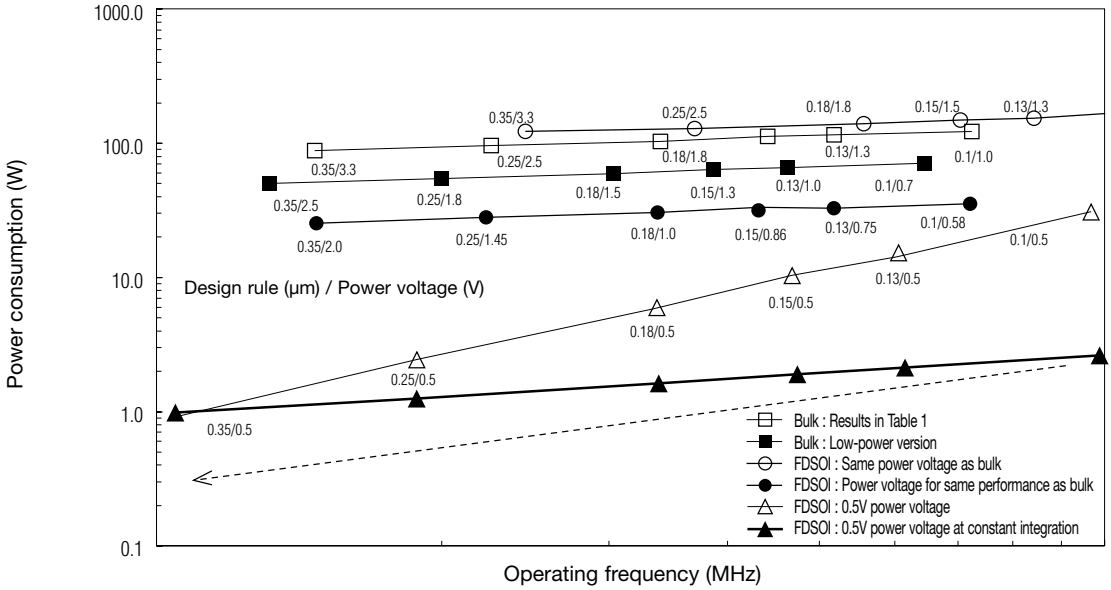

Fig. 4 Comparison of performance and power consumption

converted to FDSOI architecture, we found that the performance of the FDSOI-CMOS (○) was effectively a whole generation ahead of the bulk CMOS, at the same power voltage as the bulk CMOS (Fig.4 : □). Also, when the power voltage of the FDSOI was dropped (Fig. 4 : ●) to achieve the same performance as the bulk CMOS (Fig. 4 : □), the power consumption was approximately one third of the power used by the bulk CMOS.

In an FDSOI CMOS, further power savings can be achieved by reducing the power voltage to 0.5V.[7] In an FDSOI-CMOS, the threshold voltage can be reduced beyond that of a bulk CMOS, and since the parasitic capacitance is also low, a minimum power voltage of 0.5V can be set. By setting the voltage to 0.5V (Fig. 4: △), although the power consumption differential between the FDSOI and bulk CMOS declines with each generational advance, due to corresponding power voltage reductions in the bulk CMOS also, it is still possible to achieve two-order power savings in the 0.35 µm generation, and single-order power savings in the 0.1 µm generation. When a uniform level of integration (one million gates) was assumed (Fig. 4 : ▲), equivalent characteristics could be achieved in the 0.1 µm generation at a power level some two orders of magnitude lower than a bulk CMOS, and when the architecture-level scheme is considered, including the activation of operationally significant blocks, and the like, an LSI functioning at several Watts can be achieved.

At an operating frequency of around 100 MHz, LSI performance is adequate for image processing in a portable terminal, and therefore it was decided to reduce the operating frequency to 100 MHz in order to make further power savings. Since power use declines in proportion to the operating frequency, in the 0.1 µm generation, the power is 275 mW, and if converted to a pass transistor device, power is further cut to about 1/3, meaning that a 90 mW LSI (sub-100 mW class LSI) is achievable. Even with FDSOI technology, reducing the power voltage to 0.5V gives rise to problems with the MOS standby current, due to the reduction in threshold voltage which occurs with scaling. In this case, the standby current can be reduced by adopting a multi-threshold type circuit structure similar to a bulk CMOS. On another point, since FDSOI involves separating out the elements, then the standby current can be reduced by setting the power voltage to 0.6V or below and selecting a DT-MOS circuit system to connect the gates and bodies and control the threshold voltage dynamically. This circuit approach can be adopted more easily than in a bulk CMOS.

Conclusion

Here, we have investigated the possibility of fully depleted SOI-CMOS devices anticipated as the next generation of low-power-consumption devices, on the basis of scaling calculation models from existing bulk CMOS devices. FDSOI technology is able to make use of previous bulk CMOS design assets without any modification, whilst achieving performance which is one generation ahead of bulk CMOS performance at the same power voltage, or achieving the same performance level at a reduced power consumption of one third of the power used by bulk CMOS devices.

100 MHz operation is possible at a power voltage of 0.5V, and by adopting power saving measures in the respective areas of circuit scheme and architecture, it is possible to achieve a sub-100 mW class ultra-low-power LSI.

Appendix Calculation model for LSI power consumption and performance

In calculating power consumption and performance in an FDSOI CMOS LSI, it is necessary to estimate the level of LSI integration and the element performance. Therefore, a model based on scaling of a bulk CMOS is devised first, and this model is applied to the FDSOI technology. This section looks at the scaling model used in this paper.

In a logic LSI, the cell library is drawn up in wiring lattice units, and the level of LSI integration is calculated from the minimum interval in single layer metal. In the logic library, it is assumed that four transistors are used per gate, and the number of gates installed per chip, N_{gate}, is derived from

$$N_{gate} = A_{chip} \frac{R_{core}}{35 \cdot P_{metal}^2} \qquad \text{[Equation 1]}$$

Here, A_{chip} is the chip surface area, R_{core} is the occupation ratio of the internal circuitry, and P_{metal} is the wiring pitch in one metal layer. P_{metal} is found from the gate length L_g by design rule checking.[8]

$$P_{metal} = 2.62 \cdot L_g \qquad \text{[Equation 2]}$$

The factors required to determine transistor performance are the gate length, gate oxide film thickness, and threshold voltage. The gate length is calculated from the microfabrication process. The thickness of the gate oxide film T_{ox}, on the other hand, is indicated by the relationship

$$L_E = k \cdot T_{ox} \qquad \text{[Equation 3]}$$

with the electrical gate channel length L_E .[9] Here, k is a proportional constant, which is set to 45 [9], and it is assumed that $L_E = L_g$. Next, the maximum applied voltage V_{DDmax} can be calculated on the basis of the guaranteed voltage tolerance of the oxide film BV_{ox}, as follows:

$$V_{DDMAX} = BV_{ox} \cdot T_{ox} \qquad \text{[Equation 4]}$$

Here, the maximum applied voltage is found by setting the voltage tolerance $BV_{ox}$to 5 MV/m. The power supply voltage V_{DD} is generally estimated as follows from the maximum applied voltage, to allow a ±10% variation in power voltage.

$$V_{DD} = 0.9 \cdot V_{DD\,max}$$ [Equation 5]

It has been reported that the delay time in the CMOS circuit deteriorates sharply when the ratio of the threshold voltage to power supply voltage exceeds 1/4.[10] By setting a low threshold voltage, the leakage current at idle will rise, leading to increased power consumption when the circuit is not in operation. Therefore the threshold voltage is set by balancing performance against power consumption. Here, it is assumed that

$$V_{th} = \frac{1}{4} V_{DD}$$ [Equation 6]

and a drift current model is used for the MOS on current I_{on}.[11]

$$I_{on} = \frac{W_g}{L_g} \frac{\mu}{2n} C_{ox} (V_{DD} - V_{th})^{\alpha}$$ [Equation 7]

Here, W_g is the gate width, μ is the drift rate, C_{ox} is the capacitance of the oxide film, a is a fitting coefficient, generally set to 1 – 2 [9] [12] [13], and n is the substrate coefficient, which is calculated as shown below. [11]

$$n = 1 + \frac{\varepsilon_{si}}{C_{ox} x_{d\,max}}$$ [Equation 8]

In a bulk device, this takes a value of 1.4 – 1.6. Here, X_{dmax} indicates the width of the depleted layer.

The effective drift rate in the channel μ_{eff} is calculated using an integrated representation model [14].

$$\mu_{eff} = \frac{\mu_0}{1 + (\frac{E_{eff}}{0.75})^{\gamma}}, \quad E_{eff} \cong \frac{V_{DD} + V_{TH}}{6 T_{ox}}$$ [Equation 9]

Here, μ_0 is the carrier drift rate and E_{eff} is the effective electric field.

Next, the power consumption of the LSI chip and the operating frequency are estimated using a SUSPENS model [15] . The power consumption P_c can be derived from the total capacitance C_{tot} including the chip wiring.

$$P_C = \frac{1}{2} \cdot F_C \cdot F_d \cdot C_{tot} \cdot V_{DD}^2$$ [Equation 10]

$$C_{tot} = \frac{D_C^2 \cdot N_w \cdot E_w \cdot C_{inter}}{P_{metal}} + C_{tr} \cdot k \cdot N_{gate} \cdot F_{gate}$$

where F_c is the operating frequency, and F_d is the operating rate of the gates in the chip. D_c is the length of one edge of the chip, N_w is the number of wiring layers, E_w is the gate use rate, and F_{gate} is the average fan-out. The operating frequency F_c and the average rate delay T_{gate} can be described by the number of logic steps F_{ld}.

$$F_C = \frac{1}{F_{ld} \cdot T_{gate}}$$ [Equation 11]

$$T_{gate} = F_{gate} \cdot R_{gout} \cdot C_{inter} + F_{gate} \cdot R_{gout} \cdot C_{gin} + 0.5 \cdot R_{inter} \cdot C_{inter} + \cdot R_{inter} \cdot C_{gin}$$

In this equation, R_{gout} is the output resistance, R_{tr} is the on resistance of the transistor, C_{gin} is the gate input capacitance, C_{tr} is the transistor gate capacitance, C_{inter} is the wiring capacitance, C_{int} is the wiring capacitance per unit length, and R_{inter} is the wiring resistance.[15] These resistances and capacitances can be derived as follows from the wiring height, H_{int}, the wiring width, W_{int}, the wiring spacing, W_{sp}, the interlayer film thickness, T_{int}, the wiring resistance ratio, R_o, and the number of repeaters, k.

$$R_{gout} = R_{tr} \cdot \frac{F_{gate}}{k}, \quad R_{tr} = \frac{(V_{DD} - V_{th})}{I_{on} \cdot W_g}$$ [Equation 12]

$$C_{gin} = 3 \cdot k \cdot C_{tr}, \quad C_{tr} = \varepsilon_{ox} \frac{L_g \cdot W_g}{T_{ox}}$$

$$C_{int} = \varepsilon_{ox} \varepsilon_o [1.15 \frac{W_{int}}{T_{int}} + 2.8 (\frac{H_{int}}{T_{int}})^{0.222} + \{0.06 \frac{W_{int}}{T_{int}} + 1.66 \frac{H_{int}}{T_{int}} + 0.14 (\frac{H_{int}}{T_{int}})^{0.222}\} (\frac{T_{int}}{W_{sp}})^{1.33}]$$

$$R_{inter} = L_{av} \cdot \frac{R_o}{H_{int} \cdot W_{int}}, \quad C_{inter} = C_{int} \cdot L_{av}$$

The average wiring length L_{av} is derived as follows in units of the gate pitch d_g [16].

$$L_{av} = R_{bar} \cdot d_g, \quad d_g = F_{gate} \cdot R_{bar} \cdot \frac{P_W}{E_W \cdot N_W}$$ [Equation 13]

R_{bar} is the average wiring length in gate pitch units, and is given by the following equation using the Rent coefficient p.

$$R_{bar} = \{ \frac{(p - 0.5)}{p} - N_{gate}^{0.5} - \frac{(p - 0.5)}{(6 N_{gate}^{0.5} \cdot (p + 0.5))} + N_{gate}^{p} (\frac{- p - 1 + 4^{(p-0.5)}}{2(p + 0.5) \cdot p \cdot (p - 1)}) \} / \{ N_{gate}^{(p-0.5)} \frac{- 2p - 1 + 2^{(2p-1)}}{(2p(p - 1)(2p - 3))} - \frac{(p - 0.5)}{6p \cdot N_{gate}^{0.5}} + 1 - \frac{(p - 0.5) N_{gate}^{0.5}}{(p - 1)} \}$$ [Equation 14]

Next, the idle leakage current I_{off} when the device is at standby is found by the following equation, if the threshold voltage is defined as the gate voltage at which the drain current becomes $L/W*0.1(\mu A)$.

$$I_{off} = \frac{L_g}{W_g}\frac{0.1}{10^{Vth/S}} \quad , \quad S = n\frac{kT}{q}ln(10)$$

[Equation 15]

S indicates the gate voltage required to induce a one-order change in the sub-threshold current.

When this model was used to calculate the performance and power consumption of different generations of CMOS devices, the results shown in Table 1 were obtained. These calculations supposed a chip surface area of 10 mm^2, and the level of gate integration was determined assuming a 10% chip area occupation by the I/O circuit. The calculations were also based on figures of: average fanout 3, 40% gate use rate, 30% LSI operating rate, 25 logic steps, 9 repeaters, and a value of 1.5 for the coefficient a used to calculate the on current.

In calculating the performance of the FDSOI LSI, some corrections are applied to the junction capacitance and threshold voltage figures.

Firstly, the junction capacitance of a bulk MOS can be calculated from this formula:[17]

$$C_{jo} = [\frac{q \cdot \varepsilon_o \cdot \varepsilon_{si} \cdot N_A \cdot N_D}{2\phi_B}(N_A + N_D)]^{0.5}(1 - \frac{V_{pn}}{\phi_B})^{0.5}$$

$$C_J = [C_{ja} \cdot (bc) + Cj_p \cdot (2b + 2c)](1 - \frac{V_{pn}}{\phi_B})^{-m}$$

[Equation 16]

C_{ja} and C_{jp} are respectively the underside junction capacitance per unit area, and the peripheral junction capacitance per unit length, when V_{pn} is 0V. b is the width of the diffusion region and c is the width of the diffusion region.[sic] Since an FDSOI device is fabricated on top of a buried oxide film, the surface portion of the junction capacitance can be ignored. Therefore, the FDSOI junction capacitance is reduced to around 1/10th of that of a bulk MOS. As the SUSPENS model does not account for junction capacitance specifically, it is adjusted by correcting the average fan-out number.

Performance correction is achieved by factoring in the substrate coefficient of the FDSOI device. Taking account of the capacitance of the buried oxide film C_{box},[11] the substrate coefficient is given by

$$n = 1 + \frac{\varepsilon_{si}}{T_{si}(C_{ox}\frac{\varepsilon_{si}}{T_{si}} + C_{box})}$$

[Equation 17]

From this, in an FDSOI device, n is 1.05 – 1.1, and the S factor is 60 – 65, and these figures are reflected in the ON current calculation.

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