Development of the low-cost generic ARM MCU (ML674000) fitted with µPLAT-7B

Tetsuo Nakazawa
Koichi Takeda
Mitsunori Nakata
Osamu Nakazawa

The advance of networking between information technology machines has accelerated the expansion of functionality in related devices. These devices are facing reducing product life cycles, and require short-TAT product development enabling quick time-to-market. In order to achieve flexible and timely development in response to increased functionality and performance in system architecture, a shift is underway from specialized hardware towards software-centred processing and control. Inheritability of already developed software assets is also important increasing development efficiency, and this means that de facto standards and multi-vendor agreements for the large accumulation of software assets is desirable for the CPUs running this software.

These demands apply to many embedded devices fitted with 16-bit MCUs (Micro Controller Units), as well as existing 32-bit MCUs, while demands have been growing for a transfer to a de facto standard 32-bit RISC CPU.

The ML674000 was developed as a generic low-end ARM microcontroller for software-oriented systems of this kind. The ML674000 uses the µPLAT-7B as its CPU platform. The µPLAT[1)]-7B, a CPU platform which has specifically developed for 32-bit low-end systems, uses an ARM7TDMI*[2)] CPU.

Oki Electric has introduced ARM CPUs as its de facto standard CPU for embedded devices, and has already developed various MCU products. Oki has also designed CPU platforms (µPLAT [2)]) incorporating the minimum functions required for real-time OS operation, and has produced high-quality MCUs with short TAT. The µPLAT is one of the key elements of our SPA (Silicon Platform Architecture) design infrastructure. [3) 4)]

"µPLAT" indicates various types of platform corresponding to different applications.

The µPLAT-7C is a mid-class CPU platform comprising an ARM7TDMI equipped with a cache.

The µPLAT-7D also uses an ARM7TDMI with a cache, but gives improved cost performance.

The µPLAT-92 is a high-end CPU platform using an ARM920T CPU.

The µPLAT-7B was developed for installation in the ML674000 as a CPU platform for low-end MCUs.

Development history

As described above, the increasing shift from hardware to software-based system control applies not only to existing devices fitted with 32-bit MCUs, but also to many embedded devices using 16-bit MCUs. With this growing emphasis on software, demands have risen for a transition to de facto standard 32-bit RISC CPUs, in order to maintain software development efficiency and carry-over of software assets. However, there is virtually no choice of de facto standard generic 32-bit MCUs at entry-class level to meet the needs of those users wishing to move to these controller units from existing 32-bit MCUs or 16-bit MCUs.

In the light of this, the ML674000 was developed to meet these requirements, based on the following criteria:

- maintaining good inheritability of software assets
- reducing peripheral to the simplest possible functions, in line with the software-centred processing
- raising memory expandability.

Software assets can be carried forward by setting the de facto standard ARM CPU as the 32-bit RISC CPU for embedded devices. Most MCUs fitted with ARM CPUs are either Application Specific Custom Products (ASCP) or relatively large-scale Application Specific Standard Products (ASSP), but there are relatively few ARM-based MCUs at entry-level.

By incorporating the CPU into the µPLAT platform, excellent inheritability of software assets can be obtained, even when transferring to different MCU series which have enhanced performance due to their expanded peripheral functions or upgraded CPU platform. This is because the µPLAT is a CPU platform which has primitive OS functions built in, and the peripheral functions are virtually common to all versions of µPLAT.

Peripheral devices have been designed with software processing in mind to provide the primitive functions this processing requires. For instance, until now, embedded MCU timers have often used counter values to generate a number of external signals, but here, a timer processing function was devised to provide the time management required for software processing.

*1) µPLAT is a registered trademark of Oki Electric. *2) ARM7TDM1 is a registered trademark of ARM Ltd.

Various memory devices, such as a SDRAM, can be connected to the external memory bus. In addition to the embedded internal memory expandability which enables MCU serialization, provision has also been made for installation in a MCP (Multi Chip Package).

Overview of the ML674000

A functional block diagram and photograph of the ML674000 are shown below. (Fig. 1, Photo 1).

The ML674000 comprises a µPLAT-7B (CPU platform containing ARM7TDMI chip), an internal RAM, interrupt controller, timer, PWM (Pulse Width Modulation), watchdog timer, asynchronous serial interface, GPIO, AD converter, DMA (Direct Memory Access) controller, and the like.

The µPLAT-7B is constituted by an ARM7TDMI, interrupt controller, OS system timer, synchronous serial interface, system control section, internal ROM (or flash ROM) for processing bus connections, RAM controller, external memory controller (ROM (or flash ROM), SRAM, IO device), test interface, and so on.

An AMBA® *3) (Advanced Microcontroller Bus Architecture), the de facto standard on-chip bus for ARM CPUs, is used for the internal bus. Peripheral devices are connected to an AHB (Advanced High-performance Bus) and APB (Advanced Peripheral Bus), both AMBA® components.

An external memory controller is installed, allowing connection of a ROM (or flash ROM), SRAM, SDRAM and IO device.

Table 1 shows the features of the ML674000.

Development environment

Some of the tools used for developing the software for the ML674000 include the CPU evaluation board, Oki ADI (ARM Debug Interface), and the Software Development Toolkit, which enable evaluation and debug support of embedded systems using the ML674000 (Fig. 2).

An emulation RAM and flash memory are mounted on the CPU evaluation board to enable program execution and debugging. The board is fitted with a JTAG (Joint Test Action Group) which is the standard debug interface for ARM CPUs, and an Oki-ADI with an interface identical to Multi-ICE®*4) is connected to this interface. Program development is carried out on a PC by running the SDT (Software Development Toolkit), which provides an integrated software development environment including both compiler and debug utilities.

Serialization

The move from dedicated hardware processing to software-centred processing means that processes previously carried out by hardware logic must now be performed by software. In view of this, there is a requirement for silicon vendors to provide architectures with greater memory expandability, in order to increase software-based processing efficiency.

The µPLAT-7B mounted in the ML674000 is capable of internal memory expansion on the processor bus, to which mask ROMs or flash ROMs can be connected.

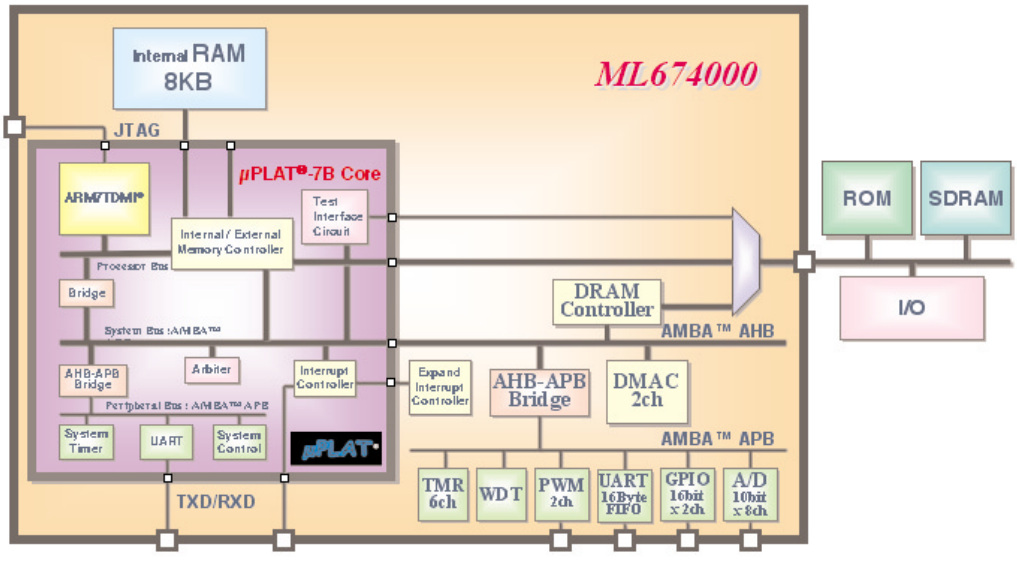

Fig. 1 Structure of ML674000

Photo 1 ML674000

*3) AMBA is a trademark of ARM Ltd. *4) Multi-ICE is a trademark of ARM Ltd.

Table 1 Features of ML674000

Operating frequency	up to 33MHz	
Internal RAM	8KB	Processor bus connection (no wait)
External memory controller	ROM/FLASH, SRAM, IO EDO/SDRAM	ROM/FLASH, SRAM, DRAM, IO bank (with wait controller)
DMA controller	2ch	Transfer mode : cycle steal / burst Address mode : dual address Transfer request : external/software Channel priority : fixed/round-robin
Interrupt controller	External cause : 5 Internal cause : 18	External cause : IRQ(4), FIQ(1) Internal cause : IRQ (18), (system timer (1), expansion timer (6), PWM (2), WDT/IVT (1), UART (1), SIO (1), AD (1), DMA (2), GPIO (2), software (1))
System timer	16bit x 1ch	Auto reload timer (µPLAT-7B)
Expansion timer	16bit x 6ch	One-shot, interval
PWM	16bit x 2ch	
WDT	16bit	Watchdog mode; interval mode
SIO	2ch	1 ch : start-stop synchronous serial interface (µPLAT-7B) 1 ch : start-stop synchronous serial interface with 16-byte FIFO
GPIO	16bit x 2ch	16bit PIO x 2ch (with interrupt function)
ADC	10bit x 8ch	
Operating voltage	Core : 2.5V(±10%) I/O : 3.3V(±10%)	
Package	128pinTQFP (14 x 14mm)	

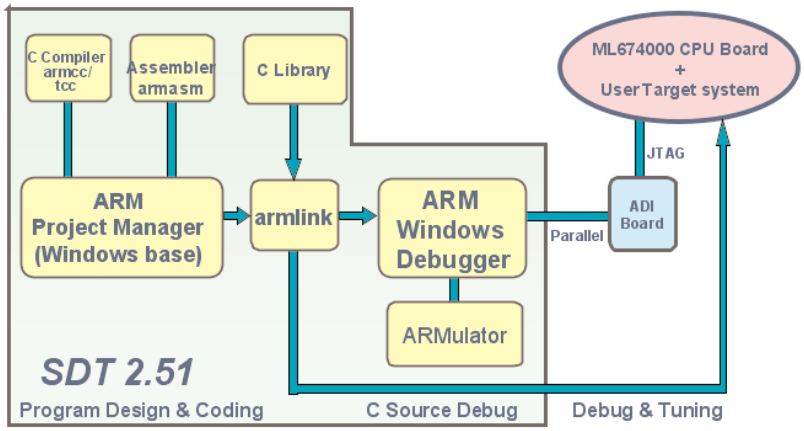

Fig. 2 Development environment

There is also a wealth of IP (Intellectual Property) compliant with the AMBA® internal bus, so functionality can easily be expanded by incorporating this IP.

In this way, the ML674000 provides increased memory and function expandability, and MCUs based on this can readily be serialized. A ML674001 expanded the function from the ML674000 and a ML67Q4002 built in a flash ROM (Fig. 3) are scheduled for future release.

We are proceeding with the development of a large number of custom LSIs based on the ML674000 and incorporating memory and peripheral functions. An example of memory/function expansion based on the ML674000 is shown in Fig. 4.

Postscript

In the ML674000, we have developed a generic MCU which is suited to software-oriented embedded systems. The new CPU platform for low-end systems, the µPLAT-7B, has been created for installation in this controller, and in the future, we will be developing other MCUs using CPU platforms (µPLAT-x) designed for a large variety of applications.

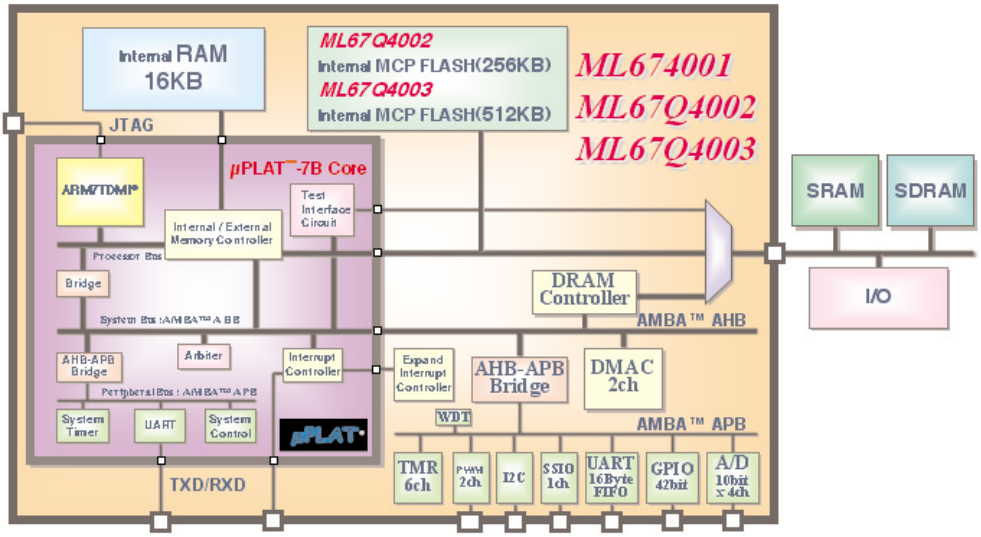

Fig. 3 Structure of ML674001/ML67Q4002/ML67Q4003

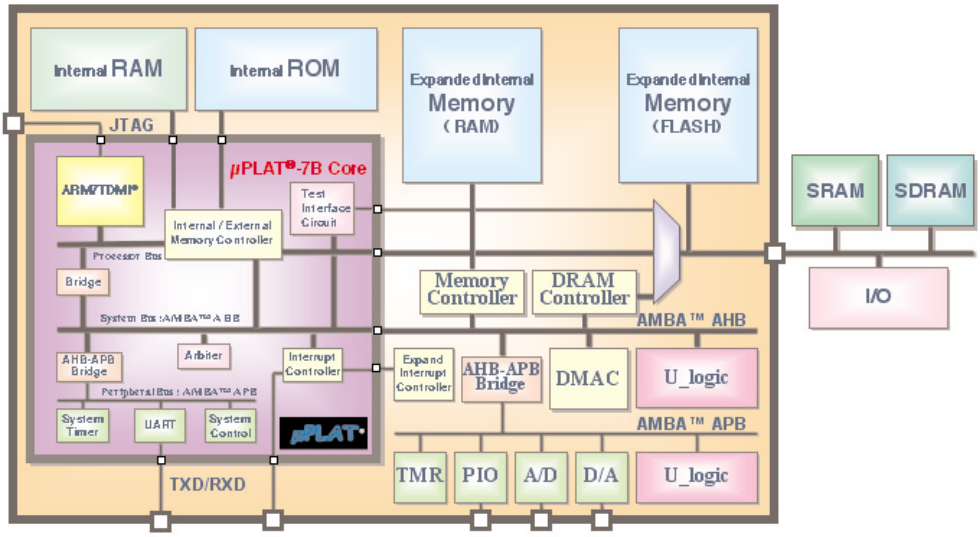

Fig. 4 ASCP/ASSP based on ML674000

References

1) Andrew Allison “Inside the New Computer Industry”, 2000
2) Kishi, Takazuka, Nakazawa : “μPLAT hardware development”, Oki Electric R&D, Issue 184, Vol. 67 No. 3, pp.45-48
3) Furuno : “Oki Electric System LSIs”, 2001 System LSI Technology Encyclopaedia, Denshi Journal Sha, pp.91-94, 2001
4) Furuno, Tomizawa : “Media SPA architecture”, Oki Electric R&D, Issue 180, Vol. 66 No.1, pp.13 – 16, 1999

Authors

Tetsuo Nakazawa : Silicon Solutions Company, LSI Div., Marketing Dept., Advanced Digital Consumer Business Unit.
Koichi Takeda : Silicon Solutions Company, LSI Div., Marketing Dept., Advanced Digital Consumer Unit.
Mitsunori Nakata : Silicon Solutions Company, LSI Div., Silicon Platform Architecture Dept., ARM Microcontroller SPA Team.
Osamu Nakazawa : Silicon Solutions Company, LSI Div., Application Software Development Dept., Development Support Systems Team.