# The µPLAT®-92 micro-platform : high speed and low power consumption for system LSIs

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The µPLAT®*1) range, based on ARM CPUs and incorporating peripheral functions, such as timers for real-time OS operations, is our basic platform for system LSI development. The high-speed low-power-consumption platform, µPLAT®-92, has been developed for use in W-CDMA (Wideband Code Division Multiple Access), PDA (Personal Digital Assistant) and other portable terminals, such as Internet devices. The µPLAT®-92" is a general term for a hardware development and integration environment typified by hard IP, the µPLAT®-92 core, comprising an ARM920T®*2) CPU and the minimum peripheral I/O devices required for OS execution, and a power management IP and prototyping board. This not only enables increased speed and reduced power use in the system LSI, but also shortens development time for large system LSIs, which are increasing in size all the time, as well as allowing the user to concentrate on his own tailor-made application developments and quality improvements.

## µPLAT®-92 development policy

In their quest for all-round size and weight reductions married with high-speed performance, many system LSI designers are working to reduce development times for ever-expanding system LSIs, whilst at the same time maintaining or improving product quality. However, they have been faced with the following, seemingly insurmountable obstacles:

- With faster operation of CPU peripherals, critical paths occur and timing design cannot be constrained;
- Power consumption increases with higher operating speeds;
- Peripheral IO/external interface circuits must be designed to suit high-speed, low-power operation and real-time OS execution (timers, interrupts).

The µPLAT was developed as a solution to these problems.

## µPLAT®-92 architecture

### (1) Hardware structure

The hardware composition of the µPLAT®-92 is shown in Fig. 1.

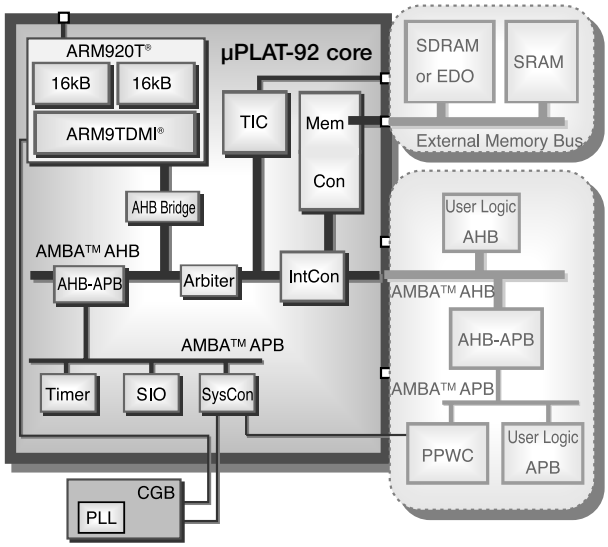


Fig. 1 µPLAT®-92 hardware structure

The µPLAT®-92 has a µPLAT®-92 core and peripheral IPs (CGB (Clock Generator Block), PPWC (µPlat PoWer Control), PDW (Power Down Wrapper), etc.). The µPLAT®-92 core comprises an ARM920T CPU (32-bit RISC processor ARM9TDMI®, 16 kB instruction cache, and 16 kB data cache), an external memory controller (MemCon), interrupt controller (IntCon), OS system timer (Timer), serial interface (SIO), system controller (SysCon) containing power management, and a test interface (TIC), etc. ARM's recommended AMBA™*3 bus is used for the on-chip buses. The AMBA™ buses include the high-speed system bus, AHB (Advanced High-performance Bus), and the medium/low-speed system bus, APB (Advanced Peripheral Bus). The AHB is used for connections to the µPLAT®-92 core.

The µPLAT®-92 core provides a 0.16 µm CMOS process hardware IP. Table 1 shows the features of the µPLAT®-92 core, and Table 2 gives a list of power management IPs.

### (2) Power Management

Power management functions are realized by power management IPs (CGB, PPWC, PDW), in

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Table 1 Features of µPLAT®-92 core (using MVt transistor)

| Item | Specification |
|---|---|
| CPU | ARM920T®<br>Processor ARM9TDM1®<br>Cache 16 kB instruction cache<br>16 kB data cache |
| External memory controller (MemCon) | SRAM, ROM, Flash ROM, I/O, SDRAM or EDO DRAM |
| Interrupt controller (IntCon) | IRQ 16 causes<br>(expandable up to 128 causes)<br>FIQ 1 cause |
| Timer | 1 channel |
| Serial interface (SIO) | Asynchronous port 1 channel |
| System control (SysCon) | Power management, etc. |
| User interface | AMBA AHB interface |
| Test interface | AMBA test interface (TIC) |
| Debug interface | JTAG interface |
| Maximum operating frequency | CPU core 133 MHz<br>AHB™ bus 66.7 MHz |

Table 2 List of power management IPs

| IP name | Functional summary |
|---|---|
| CGB<br>(Clock Generator Block) | Generates clock, controls clock gear<br>- input clock 4 switchable inputs<br>- output clock dividable 1/1 ~ 1/16<br>Constituted by HVt transistor |
| PPWC<br>(µPLAT PoWer Control) | Power down control<br>Constituted by HVt transistor |
| PDW<br>(Power Down Wrapper) | External interface of block performing power down control (based on Power OFF signal; floating of input terminal prevented) |

combination with the µPLAT®-92 core. The power management IPs are listed in Table 2.

The µPLAT®-92 has power management functions based on clock gear, individual clock halt, all clock halt and power shutdown operations, which are dynamically switchable at fine divisions of the operating clock frequency.

Software control of power management is achieved by providing arithmetic power management functions (samples) which permit easy installation of complex power management control by the user.

Fig. 2 shows a diagram of the power management architecture. If a circuit is built using a transistor of normal threshold voltage (MVt transistor), then high-speed clock operation is possible, but the current (leakage current) when the clock is halted will be greater than the high-threshold voltage transistor (HVt). In portable device applications, and the like,

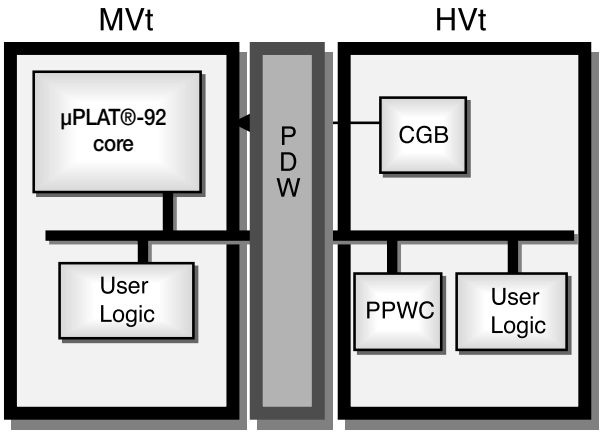


Fig. 2 Power management structure

power consumption is low at standby, but high-speed operation is required at peak use, and therefore it is very important that the leakage current is reduced.

In the µPLAT®-92, by shutting off the power to the MVt transistor block during standby, this problem is resolved and an LSI is provided which has a very small leakage current at standby, along with high clock operating speed at peak use.

## Development of the µPLAT®-92

In developing the µPLAT®-92, the following EDA tools and design techniques were used at all design stages, in order to increase design quality and shorten design time.

In the front end stage, enhanced quality was achieved by using RTL (Register Transfer Level) checkers and code coverage tools. Furthermore, to achieve generic usability, it was necessary to hypothesize certain cases, and a Specman Elite™*4) capable of random analysis was used for this. Also, in order to shorten the design time, before proceeding to the back-end stage, a synthesis tool, Physical Compiler™*5), which has excellent post-layout timing prediction capacity, was used in order to reduce rejects from the back-end. In this last phase, an SLC (System Level Constraint) flow for performing layout design using timing constraints from the front end was adopted to reduce layout rejects due to timing violations, and hence achieve early timing compression.

Emulations were introduced at an early stage to improve hardware suitability through operational checking and competition testing of all functions (normal and power management) on the OS. Fig. 3 shows a setup for such an emulation: an Aptix System Explorer TM*6) MP3C is used as the emulator, which downloads netlists from the workstation onto an

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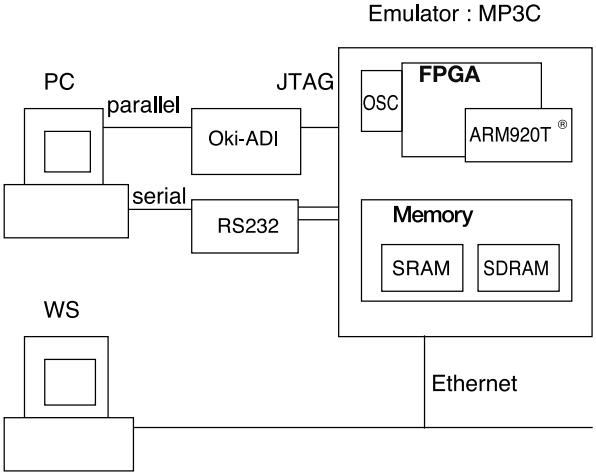


Fig. 3 Emulator setup

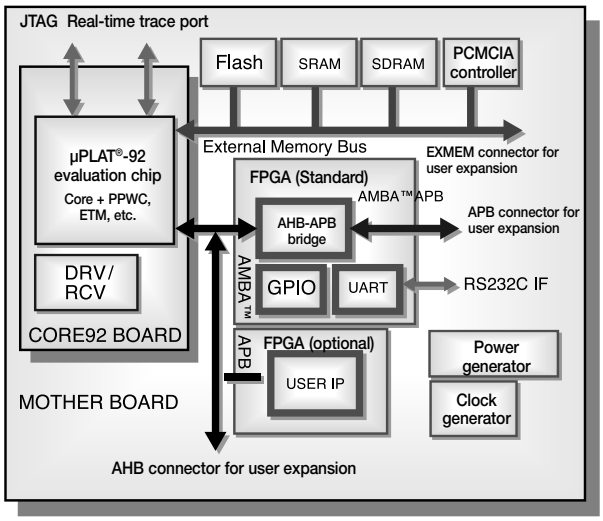


Fig. 4 Structure of µPLAT®-92 prototyping board

FPGA (Field Programmable Gate Array) via an Ethernet, and downloads a TP (Test Pattern) for analysis from a PC via a Parallel-JTAG. A Serial Port receiver for testing the internal SIO of the µPLAT®-92 is connected serially between the PC and the emulator. In this way, analysis closely simulating real operation could be carried out before wafer manufacture, helping to improve quality in the µPLAT®-92 core and shorten development time.

## Hardware development environment

### (1) µPLAT®-92 prototyping board

Fig. 4 is a compositional diagram of the µPLAT®-92 prototyping board and Table 3 shows the corresponding features of the board.

The prototyping board contains: an evaluation chip fitted with a µPLAT®-92 core, power management IP and ETM9 (Embedded Trace Macro), an FGPA (standard) containing an AHB-APB bridge connected to an AMBA™ AHB, GPIO, UART, DMAC, etc., a user FPGA (optional), and APB, AHB, EXMEM connectors forming user expansion interfaces.

A JTAG interface and a real-time trace port are provided for debugging. A PC is connected to the JTAG interface via an Oki-ADI (ARM Debug Interface Board), and hardware and software debugging is carried out by running ARM's Software Development Toolkit (SDT) on the PC.

Using this prototyping board, we have been able to install hardware circuits to be integrated into the system LSI onto the (optional) FPGA or the FPGA on the AHB/APB/EXMEM expansion boards, and analyze their functions and operations before manufacturing the system LSI (Photo 1).

Table 3 Features of µPLAT®-92 prototyping board

| Item | Specification |
|---|---|
| CORE92 BOARD | µPLAT®-92 evaluation chip |
| FPGA (Standard) | AHB-APB bridge<br>Expansion interrupt controller<br>UART<br>GPIO<br>DMAC |
| FPGA (optional) | USER IP |
| AMBA expansion | AHB expansion interface connector<br>APB expansion interface connector x 2 |
| External memory | FLASH 8MB<br>SRAM 2MB (using external ROM)<br>SRAM 1MB<br>SDRAM 16MB |
| External memory expansion | EXMEM expansion connector |
| Debug interface | OKI ADI board interface (JTAG)<br>real-time trace port |

### (2) Test bench

Fig. 5 illustrates the test bench we developed as a system LSI simulation environment capable of timing simulation for µPLAT®-92 core models and system LSI models incorporating peripheral logic.

Files compiled by the ARM SDT from test patterns created in C and assembler language, and CONF files stipulating clock frequency settings and memory attributes, are input to the test bench, which runs on a reference clock based on the same clock generator circuit CGB as that used in the µPLAT®-92. This setup permits timing simulations involving the µPLAT®-92 model, user circuit models, and IP models.

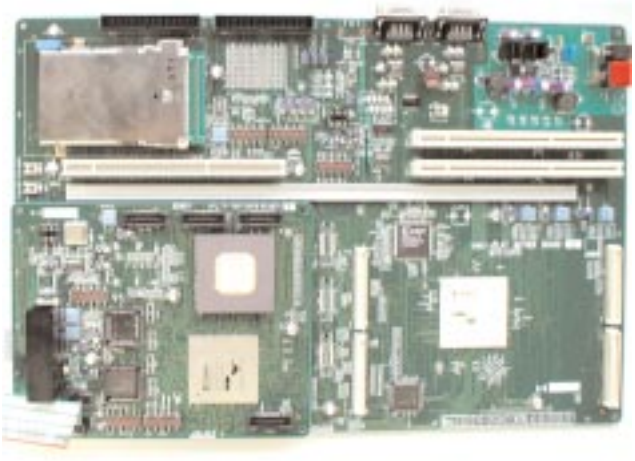

Photo 1 µPLAT®-92 prototyping board

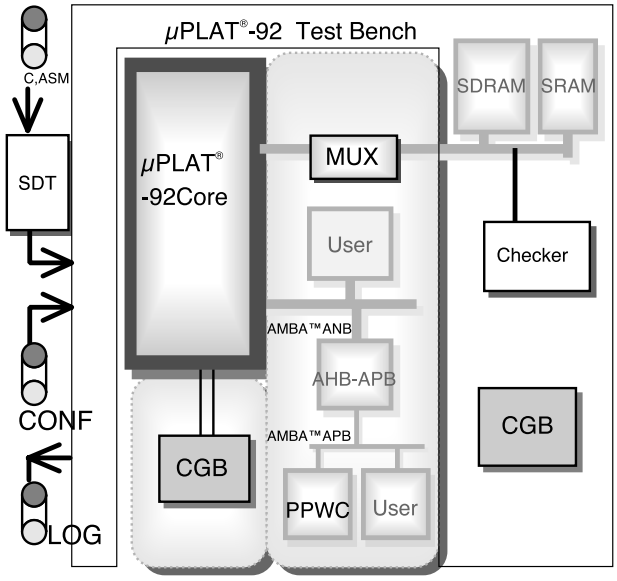


Fig. 5 µPLAT®-92 test bench

## Conclusion

This essay has presented the µPLAT®-92 core based on the ARM920T CPU, and its development environment. In the future, we aim to build system LSI products using the µPLAT®-92 core, as well as focussing our efforts on next-generation (µPLAT development and consolidation of our peripheral IP product line-up.

## References

1) Kishi, Takatsuka, Nakazawa : Oki Electric R&D, Issue 184, Vol. 67 No. 3, pp.45-48, 2000

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