Technical Development of 124-Layer PCB for Next-Generation AI Semiconductor Testing Equipment

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The Joetsu Plant of OKI Circuit Technology Co., Ltd. (hereinafter referred to as OTC) has a strong track record in advanced development/production technology for high-multilayer, high-density, large-scale printed circuit boards (PCBs). The Joetsu Plant has successfully developed a 124-layer PCB technology for equipment that performs wafer inspections of next-generation wideband memories such as high bandwidth memories (HBMs) mounted on AI semiconductors (**Photo 1**). This article describes the manufacturing and design technologies that led to the successful development of the 124-layer PCB technology.

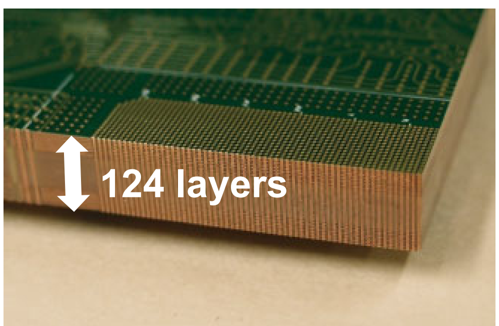

Photo 1. 124-Layer PCB

124-Layer PCB Manufacturing Technology

AI processing requires the transmission of massive amounts of data between the graphics processing unit (GPU) and memory. As GPU performance advances, the installed memory is required to provide high-speed, high-frequency, and high-density data transfers. HBM utilizes a stacked DRAM structure, which requires highly precise thinning of wafers. This in turn places higher performance and quality demands on PCBs used in inspection equipment.

The latest semiconductors handle a massive number of signals, and process miniaturization has also increased the number of chips mounted on wafers. As a result, densification and increased number of layers are required for inspection equipment PCBs in the semiconductor manufacturing process. However, various constraints limit board thickness to 7.6mm, and using conventional technology, the maximum number of layers manufacturable is 108. (**Figure 1**).

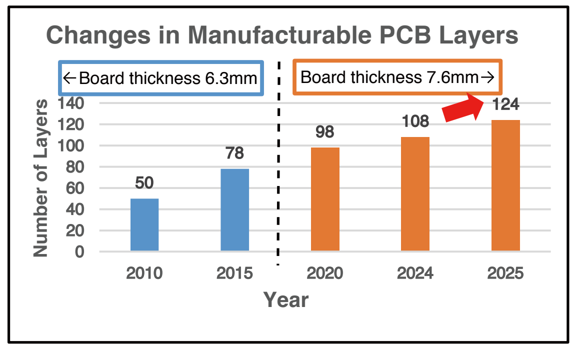

Figure 1. Changes in Manufacturable PCB Layers at OTC

To boost the 108-layer limit of the conventional technology by approximately 15% to 124 layers, OKI developed and applied ultra-thin materials and established a manufacturing process compatible with the ultra-thin materials. Details and the support specifications achieved with the developed 124-layer PCB technology are provided below.

- **Development and Application of Ultra-Thin Materials**

In order to achieve a higher layer count than the previous 108 layers of the conventional technology, it was essential to adopt ultra-thin materials that were even thinner than the conventional copper-clad laminate (CCL) and prepreg. OKI collaborated with material manufacturers to repeatedly conduct basic evaluations and high-layer PCB prototype evaluations, and after making various improvements to ensure consistent quality during manufacturing, succeeded in the development and application of ultra-thin materials.

- **Development of Manufacturing Process Compatible with Ultra-Thin Materials**

The application of ultra-thin materials also required the development of a compatible manufacturing process. As described below in (1) through (3), OKI implemented equipment, developed tooling and improved the manufacturing process.

(1) Equipment Implementation for Automated Transport of Ultra-Thin Materials

Processing of the ultra-thin materials required handling technology that provided greater precision and stability. To address this issue, OKI implemented the latest horizontal manufacturing line equipment capable of automatically transporting ultra-thin materials and worked with an equipment manufacturer to develop additional functions for automated handling of ultra-thin materials, such as loading and receiving. Additionally, the processing conditions for each manufacturing line were optimized according to the material thickness. The effort enabled the manufacturing of PCBs using ultra-thin materials. The equipment implementation was made possible through joint development of additional functions and OTC's proprietary conditional tuning.

(2) Development of Tooling Dedicated to Ultra-Thin Materials

Effort (1) described above enabled PCB manufacturing using ultra-thin materials, but further measures were needed to maintain high quality on the horizontal manufacturing line. To address this issue, new tooling was developed specifically for ultra-thin materials, enabling stable manufacturing quality and contributing to improved productivity.

(3) Improvement to Manufacturing Process of Lamination Technology

The manufacturing of ultra-high-layer PCBs using ultra-thin materials requires highly precise lamination technology to minimize misalignment when stacking layers. However, achieving this with ultra-thin materials, which are thinner and weaker than paper, presented a significant challenge. Furthermore, increasing the number of layers requires more prepreg sheets, resulting in greater in-plane board thickness variations within the PCB. To address these issues, measures such as improving the accuracy of the lamination tooling on the top and bottom of the PCB and optimizing the stacking pins to improve CCL interlayer alignment accuracy, revising the placement of the lamination tooling on the top and bottom of the PCB, optimizing the cushioning material during lamination, and revising lamination conditions (temperature, pressure) were implemented. These measures enabled the in-plane board thickness variations to be held to the same level as conventional high-layer PCBs while maintaining lamination misalignment of 70 μm or less and made stable manufacturing possible.

- **124-Layer PCB Technology Support Specifications**

Similar to the 108-layer PCBs, the 124-layer PCBs supports narrow-pitch designs down to a hole pitch of 0.5mm (**Table 1**). A cross-sectional photo of a 124-layer PCB with a hole pitch of 0.5mm is shown in **Photo 2**. Development will continue on a technology to support even narrower pitches.

Table 1. PCB Technology Support Specifications

	108-layer PCB	124-layer PCB
Board thickness	7.6mm	7.6mm
Hole pitch	0.5mm	0.5mm
Minimum drill diameter	0.2mm	0.2mm
Inner-layer copper thickness	1/2oz or 1oz	1/2oz

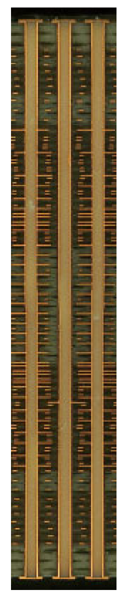

Photo 2. Cross Section of 124-Layer PCB (7.6mm Thickness, 0.5mm Pitch)

124-Layer PCB Design Technology

In order to ensure manufacturing of ultra-high-layer PCBs with stable quality using ultra-thin materials, considerations are crucial not just in terms of manufacturing technology, but for design as well. Examples are described in (1) through (4) below.

(1) SIG Layer (Signal Layer) Design

To prevent damage to the CCL substrate, SIG layer / SIG layer structures with low remaining copper ratio are generally prohibited on both the front and back of the CCL. Furthermore, to reduce the risk of laminate voids, the SIG layer should be limited to line data only, or if a coplanar structure is required, it should be designed to have a uniform remaining copper ratio across the entire CCL surface (**Figure 2**).

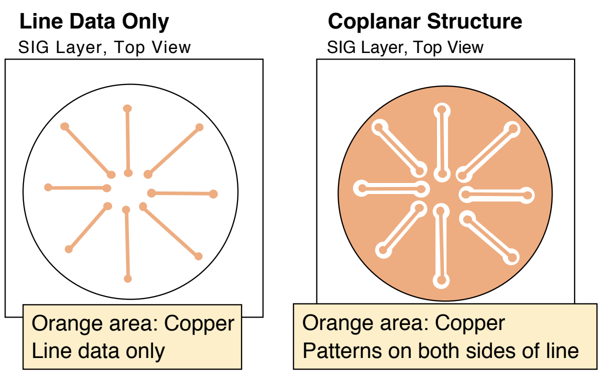

Figure 2. SIG Layer: Line Data Only / Coplanar Structure (Image)

(2) POWER Layer Design

To prevent damage to the CCL substrate, attention is given to how the power parting line is inserted.

1) When front and back of CCL are POWER layer / POWER layer

Parting lines are offset so that they do not overlap on the front and back of the CCL (**Figure 3**).

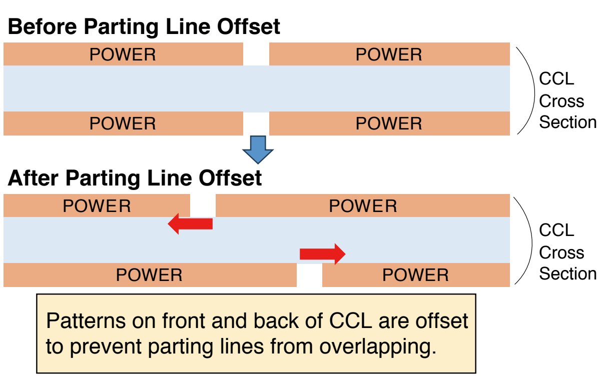

Figure 3. POWER Layer Parting Line Offset (Image)

2) When front and back of CCL are POWER layer / SIG layer

Depending on the placement of the parting lines, the strength of the CCL can be significantly reduced. Therefore, consideration is given to the remaining copper ratio and patterns on the front and back.

(3) GND Layer (Ground Layer) Design

If there are large differences in the remaining copper ratio between areas within the CCL surface, the differences will accumulate on each layer, leading to thickness variations throughout the PCB (Figure 4).

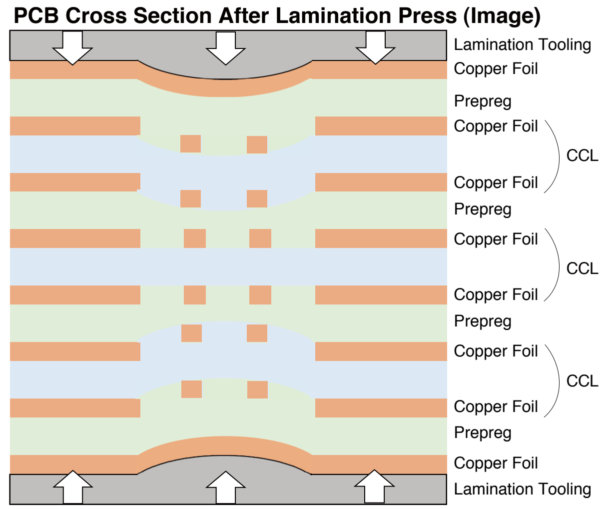

Figure 4. Differences in PCB In-Plane Thickness Due to Differences in CCL Remaining Copper Ratio (Image)

To minimize thickness variations and ensure flatness, layout should be considered so that solid patterns are not concentrated in specific areas. Also, for large-area solid patterns, measures should be taken to ensure that the remaining copper ratio is uniform with the surrounding area. (*Similarly for the SIG and POWER layers, care must be taken to ensure that the remaining copper ratio is as uniform as possible within the CCL surface.)

(4) Common Points

To prevent damage to the CCL substrate, attention needs to be given to how solid patterns are placed on the SIG, POWER, and GND layers.

1) Place a solid pattern on one side of the CCL (**Figure 5**).
2) Offset the edges of solid patterns on the front and back (**Figure 6**).
3) Chamfer the corners of solid patterns (**Figure 7**).

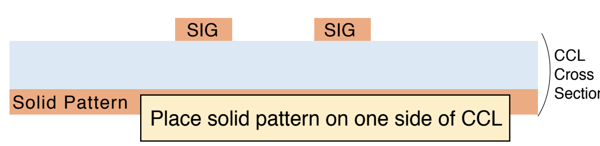

Figure 5. Solid Pattern Placement on One Side of CCL (Image)

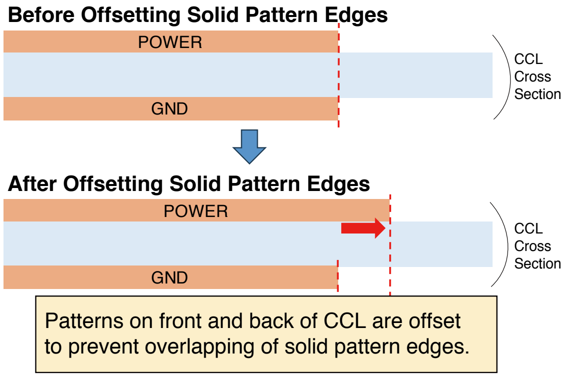

Figure 6. Offset Solid Pattern Edges (Image)

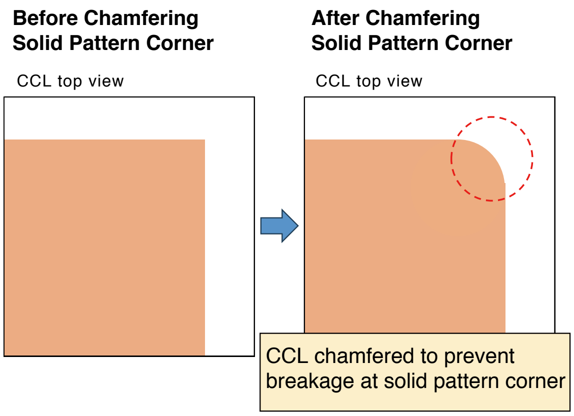

Figure 7. Chamfer Solid Pattern Corner (Image)

Conclusion

OKI Circuit Technology Co., Ltd. is focusing on developing PCB technology for cutting-edge fields expected to grow in the future, such as AI semiconductors, aerospace, defense, robotics, and next-generation communications. These fields require a variety of advanced technologies, including PCBs with multiple layers, higher density, and larger scale, as well as support for high-speed, high-capacity communications. The PCBs also need to ensure reliability and safety. Going forward, the OKI will continue to accurately grasp industry trends and client demands, and challenge itself to develop even more advanced technologies, thereby contributing to the development of society.

The development of 124-layer PCB technology was also introduced in a press release issued by OKI Electric Industry Co., Ltd. in April 2025[1].

References

1) OKI Press Release, OKI Develops 124-Layer PCB Technology for Next-Generation AI Semiconductor Testing Equipment, April 24, 2025
https://www.oki.com/global/press/2025/z25006e.html

Authors

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TIPS

【Glossary】

PCB (High-Multilayer, High-Density, Large-Scale Printed Circuit Board)
An insulating board with conductive wiring called a pattern on the surface and/or inside.

HBM (High Bandwidth Memory)
Next-generation high bandwidth memory. It consists of multiple stacked DRAMs and a dedicated high-speed interface.

DRAM (Dynamic Random Access Memory)
A temporary data storage memory widely used in computers and electronic devices. It is made up of cells consisting of capacitors that retain electric charge and transistors that control the charge. It is volatile, meaning data is lost when power is interrupted. It is capable of high-speed data read/write and is suitable for large-capacity enlargement. Example uses include personal computers, servers, and mobile devices.

CCL (Copper-Clad Laminate)
A primary material for printed circuit boards, made by stacking multiple resin-impregnated sheets on an insulating substrate (such as glass cloth), attaching copper foil to both sides, and applying heat and pressure.

Prepreg
A molded product made by impregnating a sheet or fabric of unidirectionally aligned glass fibers with a thermosetting resin (primarily epoxy resin) and dried.

Remaining Copper Ratio
A value indicating the area percentage of a pattern (area where copper remains) in the total area of the printed circuit board.

Laminate Voids
Refers to gaps (voids) that occur when the prepreg is not evenly filled between layers in PCB lamination.

Coplanar Structure
A structure in which reference lines are added to both sides of a transmission line.

Solid Pattern
A pattern in which empty spaces on a printed circuit board are filled with large areas of copper foil, such as for ground and power.