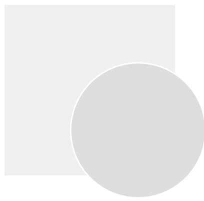

Commonization, Miniaturization, and Power-Saving Technologies for Edge Devices

Takuya Kanai

In its technology strategy announced for FY2023, OKI has set “Technology Enhancement: Edge Devices” as a key initiative (**Figure 1**) and has been working to strengthen the competitiveness of its components. Particularly in the field of edge devices, such as enterprise solutions business products, OKI is working on the “improvement of development productivity,” “multi-purpose deployment,” and “space/power savings” through core technology enhancements, moving away from individually optimized designs. This article introduces OKI’s efforts and results of technology enhancements to the base architecture promoted for enterprise solutions business based on the company’s strategic policy. Base architecture refers to both the hardware and software used commonly in edge devices.

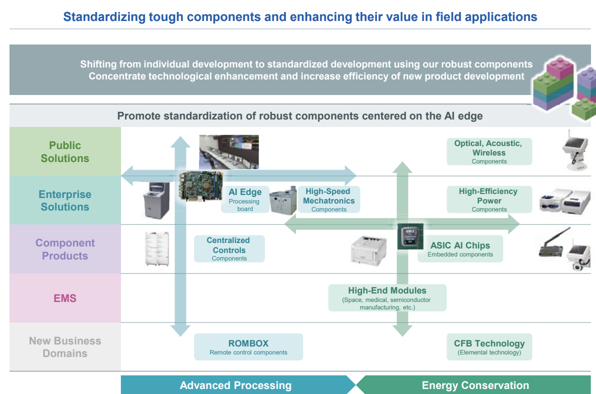

Figure 1. Technology Strategy[1)]

Development Background and Objectives

OKI’s enterprise solutions business products, such as ATMs, payment machines, and cash handling machines, have been individually optimized to meet diverse applications and needs, resulting in a wide range of product models. However, the accumulation of these individually optimized designs presented the following three issues:

- **Issue I: Inadequate Adaptability to External Factors**

  OKI’s reliance on individually optimized designs required different approaches and component procurement for each product, and the increasing component supply risks due to recent semiconductor shortages and other factors hinder the company’s ability to respond quickly

- **Issue II: Longer Product Development Periods**

  If individually optimized designs become the norm when developing products based on client requests, development periods become longer. This increases the risk of changing requirements at market launch and being surpassed by competitors.

- **Issue III: Difficulty in Deploying Environmental Technologies to All Models**

  When applying technologies for such purposes as low power consumption and reduced environmental impact, individually optimized designs and the large number of models posed obstacles, making rapid and uniform deployment difficult.

In order to address these issues for a quick and flexible response to market changes, client demands, and social responsibilities, OKI has shifted from its previous approach of individually optimized designs to a base architecture and strengthened its technological foundation.

Initiative and Technical Concepts

As solutions to the aforementioned issues, OKI is promoting the commonization of its enterprise solutions business products and evolve its circuit board technology. Previously, the mechanical control boards inside the products were individually developed to match the specifications of each product. However, in this initiative, OKI has set “commonization” of mechanical control boards as a key concept[2)] and the company focused on the following three measures.

- **Measure (1) Separated Board Configuration**

  A configuration that separates board functions into a common board and an I/O board will be adopted. This will enable component sharing, design standardization, and flexibility for functional expansion, enabling quick customization to meet client needs.

- **Measure (2) Board Miniaturization**

  A space-saving design using a multi-layer board and small components will be promoted. This will enable reuse of housings, significant shortening of development time, faster product launches, and quicker product delivery to clients.

- **Measure (3) Power-Saving Boards**

  Adoption of low-power devices and implementation of power-saving modes will be promoted. This will facilitate the deployment of environmental technologies across all models, leading to reduced operational costs for clients.

Through these measures, OKI aims to shift from individually optimized designs to a base architecture and strengthen the technological foundation (**Figure 2**).

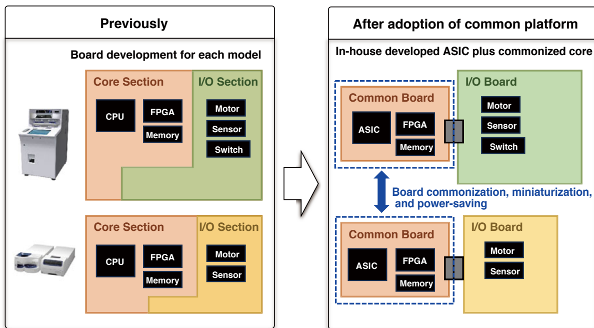

Figure 2. Base Architecture Overview

Base Architecture Configuration

This section describes the configuration and main specifications of the developed common board (**Figure 3** and **Table 1**).

The CPU mounted on the common board uses an ASIC (Application Specific Integrated Circuit) developed in-house at OKI. Additionally, the board is equipped with a FPGA (Field Programmable Gate Array) for flexible control and memory tailored to each application. USB®*1) and Gigabit Ethernet*2) are used as host interfaces, and multiple expansion interfaces (GPIO *3), LVDS *4)) are also included for scalability.

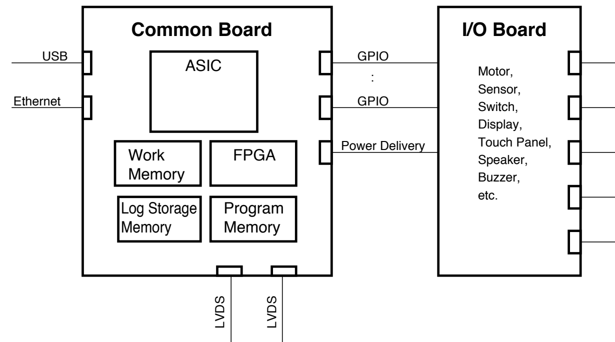

Figure 3. Block Diagram of Common and I/O Boards

Table 1. Common Board Specifications

ASIC	2 CPU cores
FPGA	I/O control logics
Memories	Work / Program / Log storage
Host interfaces	USB Gigabit Ethernet
Expansion interfaces	GPIO (general purpose I/O support) LVDS (long distance transmission support)
Power source	Single power input
Power modes	Normal mode / Power-saving mode

Measure (1) Example and Result of Separated Board Configuration

This section details a specific design example and result of a separated board configuration.

The separated board configuration, adopted as the core of the base architecture, is based on a design concept that divides the board into a common board that aggregates key functions and an I/O board that handles each model's unique functions. This approach promoted commonization of the board design, which had previously been based on a series of individual optimizations.

In the design phase, functions and requirements common in each model (control functions, communication functions, memory capacity, interface types, etc.) were identified and consolidated onto a common board. Meanwhile, model-specific functions and requirements (banknote transport control, media presence monitoring control, power supply capacity, etc.) were designed to be implemented on the I/O board. This eliminated functional overlap while creating a configuration that could flexibly accommodate individual requirements.

*1) USB (Universal Serial Bus) is a registered trademark of the USB Implementers Forum. *2) Gigabit Ethernet is an Ethernet standard established by IEEE.
*3) GPIO is an abbreviation for General Purpose Input/Output. *4) LVDS is an abbreviation for Low Voltage Differential Signaling.

The design of the expansion interface and power supply circuitry are examples of dividing functions into common and model-specific roles through board separation. The expansion interface supports high-pin-count GPIO to accommodate the assumed maximum number of I/O, and is equipped with LVDS communication to accommodate device expansion such as FPGAs, allowing for flexible support of future function additions and changes in specifications (**Figure 4**). The design aims to increase the flexibility and scalability of the base architecture to adapt to changes in business development and market needs. The power supply circuit ensures adequate capacity on the I/O board to accommodate the functional scale and operational load of each model, achieving a stable power supply without excess or deficiency. By clearly defining the roles of the common domain and the individually optimized domain, the design optimizes the balance between reliability, cost, and efficiency, enabling the value of the base architecture to be fully realized.

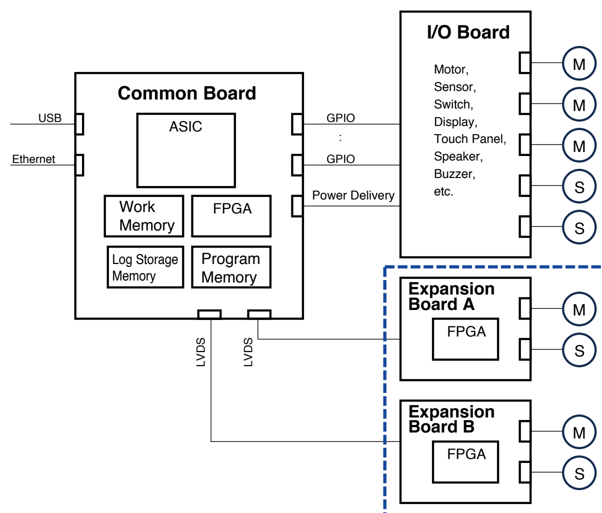

Figure 4. Example of Function Expansion using Expansion Interface

No performance degradation was observed when the common board was used in each of the model, therefore component sharing, design standardization, and flexibility in function expansion were successfully achieved. As a result, a shorter development time compared to previous products and a reduced supply risk due to stabilized component procurement are expected.

Measure (2) Example and Result of Miniaturization

This section details a specific design example and result of board miniaturization.

The previous section introduced a separated board configuration that provides efficient functional layout and support for different requirements of each model. However, increase in the number of connections resulted in a disadvantage: the overall size including the common board and I/O board increased. To overcome this issue, miniaturization of the common board was deemed critical. Therefore, design methods and implementation technologies were significantly revised.

First, the conventional four-layer board structure was switched to a multilayer build-up board, increasing the number of wiring layers and greatly improving the degree of freedom in wiring routing and integration. This made it possible to consolidate more complex and highly functional circuits onto the board in a more compact manner than before. Then, the component layout was completely redesigned and various ideas were devised to optimize the wiring pattern, resulting in a structure that allows for high-density mounting.

In the pursuit of miniaturization, it was necessary to address constraints not only in the area of the board but also in thickness. As the number of connections increased due to board separation, multiple small, low-profile board-to-board connectors were adopted to reduce overall thickness. However, there had been no previous experience of fitting together multiple board-to-board connectors simultaneously, and issues with poor fitting were anticipated due to misalignment during component mounting. Therefore, causes of misalignment were analyzed and verified in advance to confirm that there were no problems, and by reviewing the footprint and layout, both reliable fitting and high-density installation were achieved.

These efforts significantly improved wiring efficiency. However, the multi-layering and densification introduced a new issue: maintaining the quality of high-speed signal transmissions. Concerns arose that noise interference and crosstalk from nearby wiring could degrade signal quality, particularly in high-speed signal transmissions. To counter noise and ensure signal quality, the role of each signal use was clarified, GND patterns were placed on both sides of the signal pattern, and pattern width and wiring spacing were optimized. Additionally, to ensure quality from

the design stage, signal integrity (SI) simulations were performed in advance to verify not only high-speed signals but all the important signals within the common board. For the additional connections introduced by the board separation, GND pins serving as return paths were placed on both sides of the signal pins and properly connected with the board's GND, thereby enhancing noise resistance.

This multifaceted design, which took into consideration miniaturization and signal quality, overcame the issues of a separated board configuration and a miniaturized board design was achieved without sacrificing performance or reliability (**Figure 5**). As a result, wiring efficiency doubled over the previous design, while the board size was reduced to half. This enabled the effective use of equipment's internal space and reduced cost. It also provides flexibility to support multiple model deployments and specification changes, and therefore contributes to improving component competitiveness.

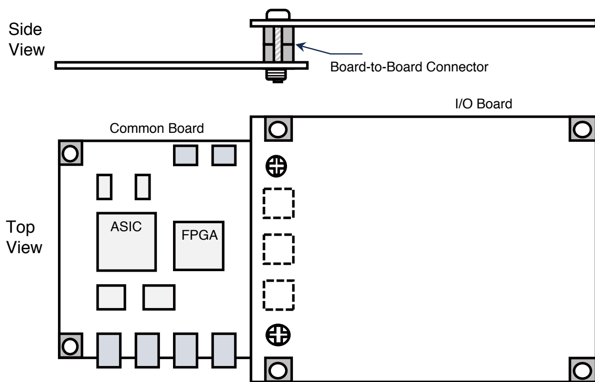

Figure 5. Diagram of Common Board Fitting

Measure (3) Example and Result of Power-Saving

This section details a specific design example and result of power-saving boards.

The previous section introduced OKI's efforts in miniaturization, but in the course of further strengthening the base architecture, it was recognized that power-saving, which would lead to reduced environmental impact and operating costs, would also be required. As society's demand for energy conservation and reduced environmental impact grows, reducing overall power consumption of equipment is also required for enterprise solutions products. In this development, power-saving was positioned as one of the pillars of the base architecture, and measures were taken on both the hardware and software sides.

Specifically, a function to control the power-saving modes was implemented using the ASIC function on the common board. Additionally, a design that controls power of both the common board, which aggregates key functions, and the I/O board, which handles the unique functions of each model, was adopted. This configuration enables flexible power-saving control tailored to operational needs.

The design allows for the selection of two operating modes depending on the use. If resume time is a priority, the common board remains powered on at all times, and only the I/O board is switched to the power-saving mode. This keeps key functions running at all times and enables quick resuming. On the other hand, to maximize power-saving, both the common board and the I/O board are switched to the power-saving mode. This de-energizes not only the I/O board but also many of the other devices mounted on the common board, leaving only the ASIC internal functions required for resuming to remain powered. This significantly reduces power consumption, but takes slightly longer to resume since key functions must be restarted. This flexible design allows optimal selection of operation for a variety of sites and equipment.

Furthermore, the switching between power-saving modes and resume timing are automatically controlled by the management software implemented on the common board in accordance with the device's operating status and external commands. This allows for fine-tuned adjustments to avoid unnecessary power consumption and minimize energy consumption during standby.

These multifaceted power-saving efforts enable power consumption to be reduced up to 80% compared to the normal mode, resulting in a significant power-saving (**Figure 6**). This also provided a technological foundation that allows for flexible selection of resuming time and power-saving effects depending on the use. The measure not only reduced environmental impact and improved client satisfaction, but also contributed to improving component competitiveness.

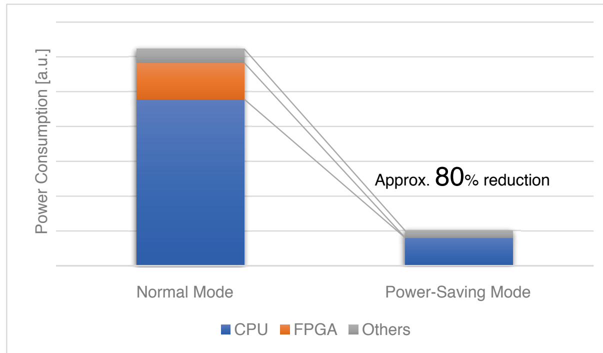

Figure 6. Effect of Power-Saving

Future Developments

In an aim to shift from individually optimized designs to a base architecture and strengthen OKI's technological foundation, focus was placed on three key initiatives: component sharing and design standardization through separated board configuration, board miniaturization and densification, and environmental impact reduction technologies such as power-saving modes. Specific design examples and their results were presented in this article.

OKI will expand these initiatives beyond enterprise solutions business to other business areas, flexibly responding to the expansion of company's overall technological foundation and the development of new functions such as AI processing technology, thereby contributing to value creation and business development across the entire OKI Group. ◆◆

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TIPS 【Glossary】

multilayer build-up board
A printed circuit board that incorporates a build-up process developed for high-density mounting.

I/O (Input/Output)
An interface for exchanging input/output signals and data.