Silicon on Sapphire (SOS) Device Technology

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The history of the development of the Silicon on Sapphire (SOS) device technology is quite old, and dates back to the 1960s[1]. SOS devices are drawing a lot of attention as they are considered to be devices that are capable of performing high-speed operations while consuming low amounts of power. However, to form the silicon (Si) layer with only small crystallization defects has been extremely difficult as there is up to a maximum of 12.5% lattice unconformity between the crystal lattice of the sapphire (Al_2O_3), which is the supporting substrate of the SOS wafer and the Si crystal lattice, as shown in Figure 1. This remained a formidable obstacle for commercializing the SOS device products and restricted all activities to research and development.

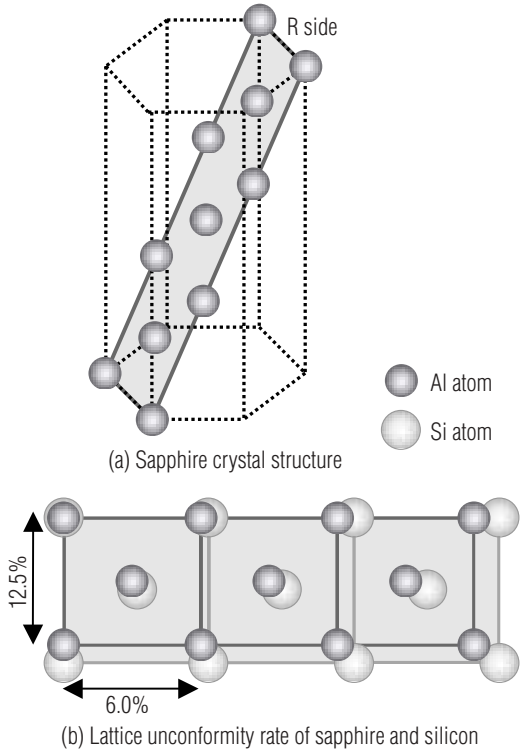

Fig. 1 (a) Crystal structure of sapphire and (b) Lattice unconformity with silicon crystal

As we entered the 1990s, Peregrine Semiconductor, of the United States, succeeded in their practical application of a technology that greatly improved the crystallization characteristics of the Si film on the sapphire substrate[2], called Ultra Thin Si (UTSi®), which resulted in an acceleration of the commercialization of SOS devices. Oki Electric implemented the SOS device technology from Peregrine Semiconductor, including this UTSi® technology and began further development of the process. Currently, both of the 0.50μm and the 0.25μm SOS processes are being developed. The 0.50μm SOS process is at the device mass production stage, while the 0.25μm SOS process is at the application to product development stage. This paper will introduce the fabricating process of the SOS devices and describe their characteristics and their advantages when compared with other devices, such as bulk Si devices

SOS wafer fabricating technology

The SOS wafer fabricating process using the UTSi® technology is described in Figure 2. Firstly, an epitaxial growth of the Si film is formed on the sapphire substrate as shown in Figure 2 (a). The condition of the deposited Si film at this time will show a lot of crystallization defects due to the lattice unconformity with the sapphire. Next Si ions are implanted inside the Si film, as shown in Figure 2 (b). This destroys the crystallization effects of the Si film near the boundary with the sapphire substrate and converts it into an amorphous condition. A heat treatment is conducted in an oxidizing atmosphere, as shown in Figure 2 (c), to form an Si film with far fewer flaws by re-crystallizing the amorphous Si film with a solid phase epitaxial growth from the Si film near the proximity of the surface with fewer flaws. The oxide film is then removed to obtain the desired Si film.

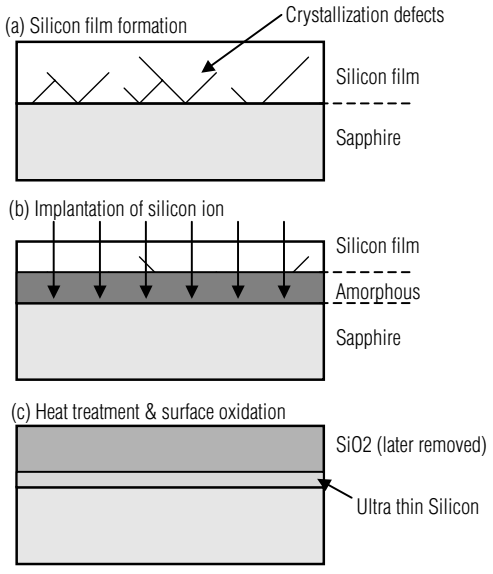

Fig. 2 SOS wafer fabricating flow

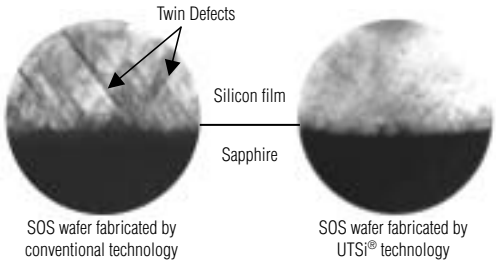

Fig. 3 Transmission electron microscopic photograph[3] of a cross section of an SOS wafer

A transmission electron microscopic photograph of a cross section of the SOS wafer is shown in Figure 3. Conventional SOS wafers contain many crystallization defects, primarily those known as "Twin Defects". It is possible to verify that with the SOS wafer fabricated using the aforementioned UTSi® technology, a favorable Si film can be formed with much fewer crystallization defects. By using the UTSi® technology, it has become possible to form Si films on sapphire substrates with a superior crystallization, even when the formed film is about as thin as 100nm.

Structure and fabricating process of the SOS device

A transmission electron microscopic photograph of a cross section of the SOS device is shown in Figure 4. The SOS device is fabricated by forming a metal-oxide semiconductor field-effect transistor (MOSFET) on the Si film located on top of a sapphire substrate, which is an insulator, as shown in Figure 5 (a). Since elements are formed on top of insulating substrates, the footprints of the source and drain, or the junction capacitance, is structurally extremely small. Further, it is also possible to completely isolate individual elements by using element separations, such as the local oxidation of Si (LOCOS). Therefore, the structure will be simple and small, making it unnecessary to form well regions of a low impurity concentration, essential for bulk Si devices as shown in Figure 5 (b).

A comparison of structures from the aspect of layout design is shown in Figure 6. The element separating distance between the NMOSFET and PMOSFET can be reduced because the well region is unnecessary with SOS devices, as described above. Further, since there is no need for a contact to stabilize the electric potential of the well region, it is easier to improve integration with SOS devices than bulk Si devices.

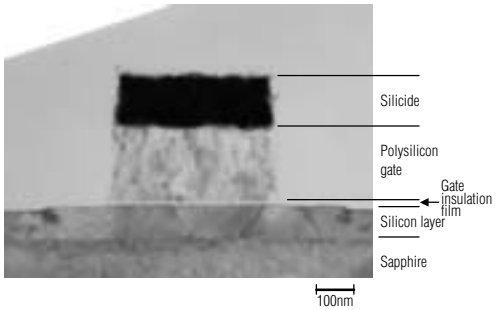

Fig. 4 Transmission electron microscopic photograph of a cross section of an SOS MOSFET device

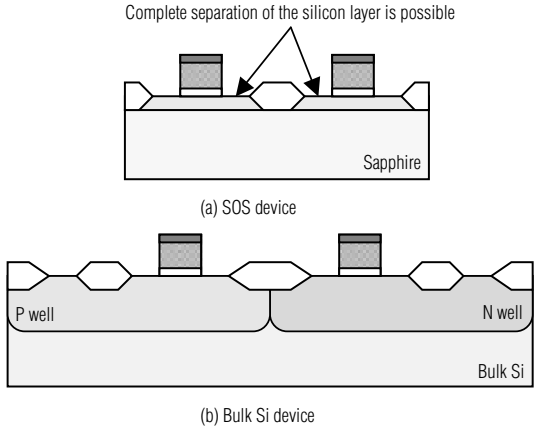

Fig. 5 Comparison of a MOSFET cross sectional structure of an SOS device and bulk Si device

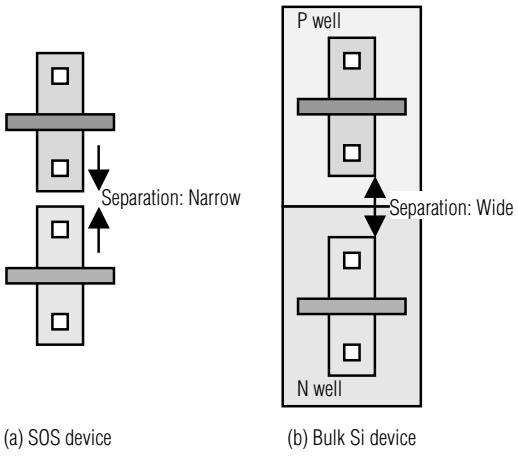

Fig. 6 Comparison of layout structures of an SOS device and bulk Si device

The fabricating process flow of an SOS device is described, in Figure 7. Firstly, an element-separating region is formed with LOCOS, as shown in Figure 7 (a). The process continues with the individual injection of impurities to determine the threshold voltage, Vt, as shown in Figure 7 (b). Next, the gate electrodes are formed as shown in Figure 7 (c). Once the sidewalls have formed, as shown in Figure 7 (d), impurities are injected to form the source and drain regions. Then contacts are formed and wired to form the desired circuitry (Figure 7 (e)).

The SOS device fabricating process described here, is the same as for the SOI device fabricated by forming the MOSFET on the Silicon on Insulator (SOI) substrate, which is fabricated by forming an embedded oxide film layer and thin Si layer on the silicon substrate. Oki Electric previously perfected the completely depleted-type SOI device technology with a history of applying this technology to the fabrication of ultra-low power consuming LSI. The SOS device technology has a great affinity to this SOI device technology.

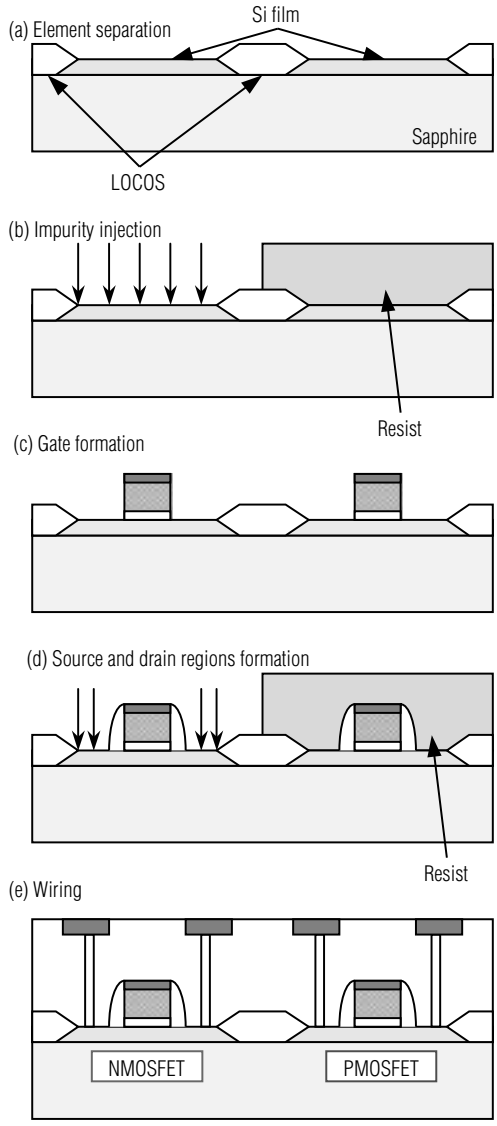

Fig. 7 Fabricating process flow of an SOS device

Thus, the fabrication of SOS devices, as described above, can be carried out similar to that of the SOI devices by utilizing the same equipment used for bulk Si devices and by applying the bulk Si device process, which already has a proven history.

Characteristics of the SOS device

The I_{ds} - V_{gs} characteristics of the SOS device are shown in Figure 8. It is possible to evaluate the amount of change of V_{gs} necessary to add one digit to I_{ds} , or the sub-threshold characteristics (S value) from the I_{ds} - V_{gs} characteristics. Smaller S values represent more superior characteristics. The S values of the SOS devices show favorable characteristics, with 70mV/decade for NMOSFET and 71mV/decade for PMOSFET. Further, since bulk Si and partially depleted-type MOSFET in general, indicate values of about 85mV/decade, it is believed that the SOS device runs a completely depleted operation.

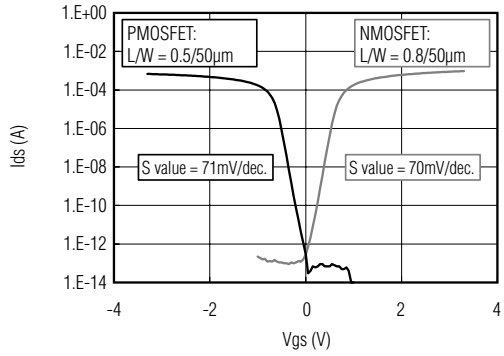

Fig. 8 I_{ds} - V_{gs} characteristics of an SOS MOSFET with a gate length of 0.5µm

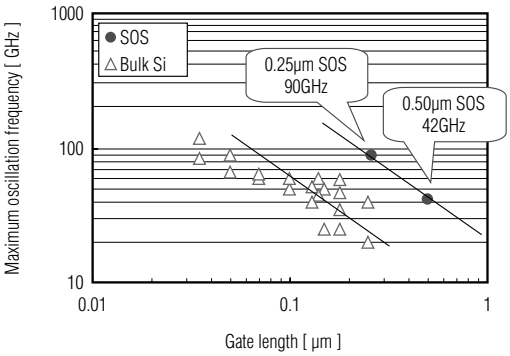

Fig. 9 Transistor high frequency characteristics of an SOS device and a bulk Si device

A comparison diagram for the transistor high frequency characteristics of an SOS device and a bulk Si device is shown in Figure 9. The performance of the transistors can be directly compared with their high frequency characteristics, by observing the maximum oscillation frequency (F_{max}). With the SOS device, F_{max} = 42GHz can be attained with a gate length of 0.50µm at 90GHz and above with 0.25µm. The F_{max} of an SOS device is approximately four times that of a bulk Si device.

The high frequency characteristics of passive elements are compared using the Q value (Quality Factor) of inductors. Q values represent the energy loss, with higher values representing superior characteristics. An example of the Q value of the fabricated inductor and the frequency characteristics of inductance L is shown in Figure 10. The Q value is 8.7 for 1.7GHz with a bulk Si device, while a Q value of 14.7 was attained for 6.5GHz with an SOS device. Since the passive elements of SOS devices are fabricated on insulating substrates, higher Q values than those of bulk Si devices, can be obtained in the high frequency range.

Features of the SOS device

Summarizing the features of SOS devices:

- Completely depleted-type MOSFET transistor.
- Complete separation of elements is possible.
- Junction capacitance is extremely small, which benefits high frequency performance and low power consumption characteristics.

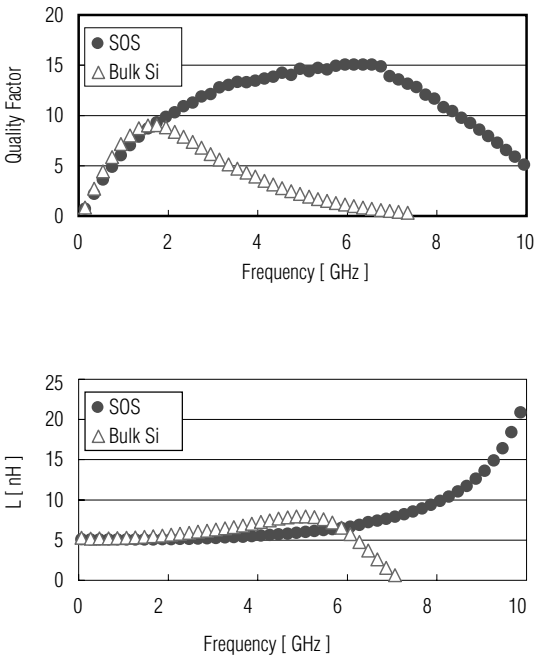

Fig. 10 Comparison of high frequency inductance characteristics of an SOS bulk device and a bulk Si device

- Realization of high performance passive elements (such as inductors).
  Further, since they are based on sapphire substrates, they have:
- Extremely high radiation resistance.
- Low crosstalk.
- Clear state of elements after the completion of a process.

These can be mentioned as beneficial features as well.

A comparison of features between the SOS device, bulk Si, SOI, Bi-CMOS and gallium arsenide (GaAs) devices, are shown in Table 1. Since the SOS device is fabricated on top of a sapphire substrate, which is a completely insulating substrate and a completely depleted operating MOSFET, it has advantages in terms of high frequency performance and low power consuming characteristics. Further, since it is also possible to fabricate passive elements with higher Q values, such as an inductor, there is a vast advantage over other types of devices.

Table 1 Comparison of various device characteristics

	SOS	Bulk Si	SOI	Bi-CMOS	GaAs
High frequency performance	◎	△	○	◎	◎
High Q inductor	◎	×	○	×	○
Integration	△	◎	◎	○	×
Lowe power consumption	◎	△	◎	×	×
Cost	△	◎	△	△	×

Then again high integration and the large areas of chips, such as those of bulk Si or SOI devices, are currently not possible since the flatness of the surfaces for sapphire wafers are somewhat inferior. Even when the UTSi®[1)] technology is used and the quality of SOS wafers are improved significantly, a few lattice defects still remain. Further, the cost of a large-diameter sapphire wafer is extremely high, which is a factor that will raise the device's cost. These issues, however, seem to have been solved and the further advantages of SOS devices are secured as the demand for SOS devices increases and improvement of SOS wafer quality, as well as a reduction in costs, occur.

Conclusion

Existing fabricating equipment, used for producing bulk Si devices, can be used for the production of SOS devices as well. SOS devices can also be fabricated by using the proven bulk Si fabricating process. Further, it is possible to implement a higher integration than with GaAs devices and advantages exist over bulk Si or SOI devices in terms of higher frequency performance and lower power consumption. Furthermore, it is possible to fabricate passive elements, such as inductors, with greater high frequency characteristics than those of bulk Si or Bi-CMOS devices.

We are currently developing these products for communications, but in the future we expect there will be many more applications that utilize the advantages of high frequency performances with low power consumption characteristics. Further, because the sapphire is clear, it is possible to use these devices in modules with a mixed load of optical devices as well. We believe that SOS devices, with these advantages, will become key devices for the ubiquitous era.

References

1) H.M. Manasevit and W.I. Simpson: "Single-Crystal Silicon on a Sapphire Substrate", J.A.P., Vol.35 pp.1349-1351, 1964.
2) M.L. Burgener and R.E. Reedy: "Minimum Charge FET Fabricated on an Ultrathin Silicon on a Sapphire Wafer", United States Patent No.5,416,043, 1995.
3) Y. Nagatomo and R.E. Reedy: "Latest Trends of SOS (Silicon on Sapphire) Technology", Denshi Zairyo, Vol. 42, No. 5, 2003.

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