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New LSI Packaging and Future Trend

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Abstract

As communication information networks expand, the mobile information terminal device market is growing rapidly. In this IT society, the key point is how to respond to changing customer needs quickly, yet flexibly. There will also be diversifying demands for the LSI package. Figure 1 illustrates a road map for LSI packages. LSI packages are expanding from insertion mounting to surface mounting, from peripheral pins to area pins, and from single chips to multiple-chip stacks. The operative key words are smaller, lighter, higher performance, and multiple-chip stacks.

In this article, we would like to introduce Oki’s newest packages and our forthcoming mounting technology for the personal and mobile markets. We developed FBGA using wire bonding technology, wafer level CSP, and chip stack MCP in our concept of small, light, and low-cost. Also, we would like to discuss the development status of our electronic system integration technology, which is a forthcoming mounting technology.

Wire Bonding Joint FBGA

This package uses solder balls as the external pins, which are arranged into a grid on the rear face of the package. The FBGA (Fine Pitch Ball Grid Array) we are developing has the following characteristics.

First, this package uses a rigid substrate as the interposer. Compared to packages that use tape, there is a slight cost disadvantage mass-producing a limited number of models. However, low cost can be realized when the models are changed frequently and a large number of models is produced in smaller lots.

Next, wire bonding joints are used as the internal connection method as in previous packages. Lead joints and flip chip joints have a small degree of connection freedom, so since an interposer design is required for individual chips, we fear that the development TAT will be long and the cost will increase.

Additionally, the packaging method used on this FBGA was to seal the package by molding it together then saw cutting it. With previous packaging methods, molding dies or dies for individual pieces were necessary when the package size or pin count differed. By employing this method however, it was no longer necessary to manufacture a new
molding die for each package. With the FBGA package, the package should be made as small as possible and the outer size is standardized with a 1.0 mm pitch. Consequently, a large number of package types existed and a molding die was necessary for each package, but with this new method a substantial reduction in facilities investment and development TAT was realized. Saw-cut packages have the additional advantage of being able to be made 25% smaller than previous packages. (See Figure 2.)

As mentioned above, the Oki FBGA package is a low-cost, highly flexible LSI package made possible by a new manufacturing method that can respond to rapidly changing market demands.

**Wafer-Level CSP (W-CSP)**

The W-CSP (Wafer-level Chip Size Package) is a new concept package in which the entire assembly process is completed at the wafer level. Similar to the FBGA package, this package has pins arranged into a grid on the rear face of the package. In contrast, the package size is the real chip size, which is exactly the same size as the chip. It could be said that this is the ultimate small package.

Figure 3 illustrates the cross-section structure of the W-CSP package. Peripherally placed bonding pads for general LSI chips are replaced and rerouted by the metal plating film. This replacing and rerouting increases the pin pitch to one that makes it easier for the customer to mount boards. Solder balls (or solder coats) are connected to the pins, but metal tower posts (plating layer) have been placed under the solder balls (or solder coats). Furthermore, the upper face of the chip has been sealed in an epoxy resin.

The above structure has the following characteristics.

1. Similar to previous packages, stand-alone quality assurance is possible

   If the pin pitch is narrow (around 0.25 mm) in high-speed tests and during burn-in, then the cost of probes for measuring the electrical characteristics and the sockets will become very expensive. Since the pin pitch of this package makes it possible to inexpensively take measurements, it is possible to inexpensively test at the wafer level. Also, the chip is sealed in a high-quality resin so that no special process is required during flux cleaning after the board is mounted. This structure also protects the chip from mechanical damage from an outside source. As a result, this package can completely guarantee quality at the stand-alone level even though it has the same dimensions as the chip.

2. Similar to previous packages, batch reflow is possible

   This is a package that allows the implementation of general batch reflow (SMT technology: Surface Mount Technology) without using an expensive special mounting method like using a flip chip bonder in the clean room. Based on the current SMT technology and the capability of motherboards, we are using a pin pitch of up to 3 rows at a 0.5 mm pitch. We plan to shift to a 0.4 mm pitch when inexpensive high-density printed circuit boards are developed. Also, in order to secure solder joint reliability after reflow mounting, we employed metal tower posts and have made the solder ball diameter a little larger. Compared to the previous flip chip method in which solder was directly connected to a silicon chip, we were able to considerably improve solder contact reliability after mounting the board.

3. Less expensive package than previous packages

   We established a low-cost process that avoids using precise, yet expensive devices such as steppers and sputters. Specifically, this process uses electrolytic plating to replace the pads and form metal tower posts. Since precision at the 10 μm level is sufficient to perform these steps, no highly precise process is required. It is known that using the electrolytic plating method can cut the process cost in half compared to the sputter film method used in flip chips for example. Of course, expensive CMPs and dual damascenes are not used either.
Another major characteristic of W-CSP is being able to perform the entire assembly process at the wafer level. Current semiconductor manufacturing lines are divided into two broad processes: wafer processing (WP) and assembly processing (AP). In the case of W-CSP however, consistent manufacturing is possible. Since the concept of this manufacturing method is completely different from that of conventional assembly plants, the production organization and production structure can be innovatively reformed.

Figure 4 illustrates the results of a comparison between existing packages such as TQFP or FBGA and W-CSP. This figure shows that the W-CSP package is most advantageous with respect to weight and mounting area. W-CSP is obviously a differentiated technology that can easily realize the small size and light weight required in mobile devices.

Oki and Casio Computer Co. Ltd. established a joint development company (IEP: Integrated Electronics & Packaging Technologies, Inc.) to develop this W-CSP technology. IEP continues to further development of the W-CSP technology and grant W-CSP technology licenses. Furthermore, IEP is accepting W-CSP fabrication consignments and has already received inquiries from several semiconductor manufacturers.

**Chip Stack MCP**

The chip stack MCP (Multi-Chip Package) is a package that can mount multiple chips within a single package. The QFP package also has an exterior contour, but the FBGA type is the main type. The outer appearance of these packages is exactly the same. (See Figure 5.)

Similar to the FBGA, the manufacturing method of the MCP employs saw cutting after molding all of the package parts together. We developed the three following technologies in order to realize this package.

The first technology is thin wafer handling. In order for the chip thickness to be the same as previous chips (300 μm) even after stacking wafers, it is necessary to shave off 150 μm thick wafers. We therefore developed the technique of wafer handling all processes while the wafers adhere to adhesive tape.

The second technology we developed is applying tape-like adhesive to the stacking adhesive (also used as die adhesive). We employed a method of applying this tape and cutting it along with the wafers before scribe partitioning them. This makes it possible to prevent misalignment between the die adhesive and the chips.

The third technology we developed is wire bonding between the upper and lower chips. Employing this technology makes it possible to facilitate signal transmission between the upper and lower chips and reduce the number of pins required for the package (thereby reducing cost).

Since two chips are contained within a single package, it is possible to mount chips more densely than when using two packages. Previously, higher two-dimensional density was attempted by making the pin pitch of the package finer. If too fine a pitch was used however, the customer would have difficulty mounting onto boards. Stacking chips made it possible to achieve a higher three-dimensional density.

This package’s function as a System in Package (SiP) is also important. A method of combining device systems onto single chips (SoC: System on Chip) in mobile devices has been proposed. When using a flash memory or mixed DRAM process however, there are cases in which the costs are higher and the to-market TAT is longer. Newly developing a mixed process not only incurs large development costs and consumes much time, but also lengthens the overall wafer process and tends to cause reduced production yield. It is generally true that the DRAM mixed process was developed for the 0.5 μm generation and the flash mixed process was developed for the 1.0 μm generation, therefore being developed later than the general CMOS processes. In the mobile information market where technical innovation is most intense, it is important to incorporate the newest transfer techniques and quickly get products out on the market. Instead of developing leading-edge mixed process chips from the beginning, there are many cases where it is advisable to use existing flash memory and low-cost DRAM as sub-chips and use the leading-edge process to develop the main chip. Chip stack MCP is a new mounting technology that will complement later SoCs (System on Chip).
Forthcoming Mounting Technologies

As illustrated in Figure 1, high-speed performance and 3-D structure will become the key technologies for the forthcoming mounting technologies. We are currently participating in the Association of Super-Advanced Electronics Technologies (ASET) that is promoting the research and development of these technologies.

Since semiconductor devices will continue getting faster, figuring out how to draw the best performance out of them will be important. Currently, we can already see devices whose internal operating speed is such that signals can be transmitted at more than 1 GHz. At the board level of electronic devices including LSI packages however, operation is no more than 300 MHz, so this high-speed performance is not being sufficiently drawn out. The signal transmission distance at the board level is 30 cm, so it is difficult to compensate for the occurrence of signal delays, impedance (waveform distortions due to reflection) or EMI (Electro-Magnetic wave Interference). From that perspective, system integration technology that realizes high-speed performance of the entire electronic device at low-cost becomes necessary. (This is referred to as Electronics SI (Electronics System Integration) technology.)

With respect to high-density mounting on the other hand, three-dimensional chip stacking technology is a must. By realizing W-CSP, increasing density in two dimensions had reached its limit. Three-dimensional packaging will be the next high density mounting technology. Three-dimensional chip stacking using penetrating contacts formed in silicon can considerably reduce the signal transmission distance between LSI chips, and is also advantageous in high-speed signal transmission.

Opto-electronics packaging technology will be important in further speeding up signal transmission since it will be able to go beyond the high-speed signal limitations of electricity. This will be a technology with which three-dimensionally stacked chip modules will be interconnected by optical wave-guide substrates or optical space transmission. (See Figure 6.)

Environment-friendly mounting technology will also be important to preserve the environment on a global scale. Such mounting design must conserve resources and promote recycling while not using materials that have a negative impact on the world environment. Currently, there is a trend toward using lead-free LSI package pins, eliminating the flame retardants used in sealing resin and organic PCBs, and stopping the use of halogen. In the future we will also address the issues of how to eliminate mutant substances and environmental hormones.

Conclusion

In this article we introduced mounting technologies relating to the newest LSI package and the forthcoming development trend. We will continue developing semiconductor packages that have high quality at low cost, are easy to use, and allow our customers to quickly respond to market trends.

References