Special Edition on 21st Century Solutions

SOI-CMOS Device Technology

Yasuhiro FUKUDA*, Shuji ITO**, Masahiro ITO**

Abstract

In recent years, the mobile communication market represented by the mobile telephone has been showing remarkable growth. This market has been making tough demands for semiconductor integrated circuits, which are mounted components, to consume less power, have higher integration, have multi-function capability, and be faster. We at Oki have been working on developing complete depletion type SOI devices in order to meet these needs. We have already implemented 0.35 µm and 0.2 µm SOI-CMOS devices[1]. This article explains SOI-CMOS device technology and discusses current developments.

SOI Device Structure

The term SOI means Silicon On Insulator structure, which consists of devices on silicon thin film (SOI layers) that exists on insulating film. Figure 1 illustrates an outline sketch of bulk, partial depletion type and complete depletion type SOI-MOS (Metal Oxide Semiconductor) transistor structure. In the case of bulk CMOS devices, P/N type MOS transistors are isolated from the well layer. In contrast, SOI-CMOS devices are separated into Si supporting substrate and buried oxide film (BOX). Also, these devices are structured so each element is completely isolated by LOCOS (Local Oxidation of Silicon) oxide film and the operating elements area (called the SOI layer) is completely isolated by insulators. Also, elements that have a thin SOI layer (normally <50 nm) and have all body areas under the channel depleted, are called complete depletion type SOI. Conversely, elements that have a thick SOI layer (normally >100 nm) and have some areas at the bottom of the body area that are not depleted, are called partial depletion type SOI.

Characteristics of SOI-CMOS Devices

As indicated below in Table 1, the S value that indicates the sub-threshold characteristics is unique in that only the S value of complete depletion type SOI transistors is the low value of 60 - 70 mV/dec. (The S value is the gate voltage at the sub-threshold area that changes the drain current by one digit with the drain voltage held constant.) Also, as illustrated in Figure 1, the source, drain, substrate, and the PN junction formed between wells in bulk transistors do not exist as complete depletion type transistors. Also, the junction capacity is very small. Since a PN junction exists at the bottom of the body in partial depletion type transistors, it is located exactly between them. The advantages of the S value, reduced junction capacitance, and the totally isolated structure are as follows.

1. A low operating voltage is possible since the threshold voltage (Vt) can be set low without increasing the off-leak current. (Reduced S value)
2. Development of high-speed, low power consumption CMOS devices is possible since the load capacitance CL is reduced. (Reduced junction capacitance)
3. Reduced signal transmission loss during high-speed operation. (Reduced junction capacitance)
4. Realizing high-frequency component performance, including passive devices, is possible since high-resistance Si wafers can be used as supporting substrates. (Totally isolated structure)
5. Reduced operation errors such as cross talk via the substrate. (Totally isolated structure)
6. It is possible to prevent operation errors including latch up phenomena. (Totally isolated structure)

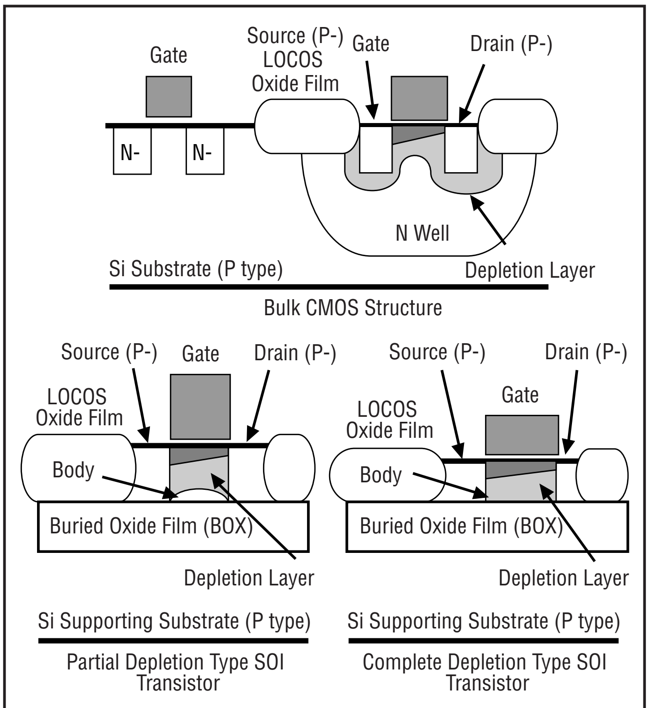


Figure 1: Comparison Between Bulk CMOS and SOI-CMOS Structures

* Silicon Solutions Company, VLSI R&D Center, Advanced VLSI Device/Process R&D Dept.-1, General Manager
** Silicon Solutions Company, VLSI R&D Center, AdvancedVLSI Device/Process R&D Dept.-1, SOI Circuit R&D Team-2, Team Leader

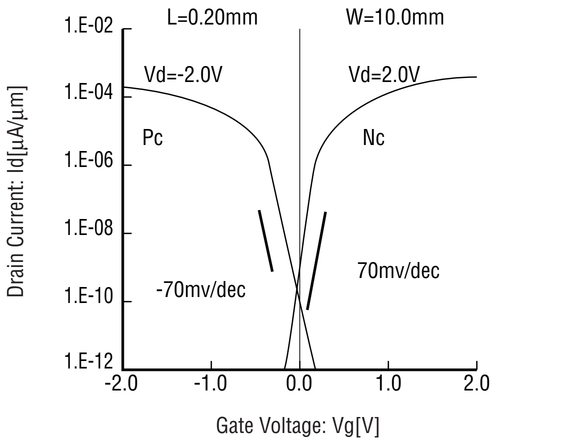


Figure 2: 0.2 μm SOI Transistor Sub-threshold Characteristics

7. Improved soft error durability by injecting radiation. (SOI layer thin film)

Since we are considering expanding into the mobile communication market, we are aiming to develop one-chip low power consumption CMOS-LSI with combined analog and digital logic. We have therefore adopted complete depletion type SOI structure transistors as our development of low power consumption devices that use the low S value to make low power operation possible. On the other hand, the following issues accompany complete isolation or thin-film SOI layers.

1. Source drain withstand voltage reduced by parasitic bipolar transistor operation (floating body potential effect due to complete isolation)
2. Increased transistor parasitic resistance (thin-film SOI layer)
3. Reduced tolerance to electrostatic discharge (ESD) (thin-film SOI layer)

Next we would like to introduce the performance of 0.2 μm SIO-CMOS devices we developed using complete depletion type SIO structure transistors to overcome these issues and take advantage of the previously mentioned advantages.

0.2μm SOI-CMOS Device Development

We developed 0.2 μm SOI-CMOS devices by stipulating the power supply voltage specifications to be 1.8 V. In consideration of the complete depletion type transistor characteristics and the current wafer variations, we specified 50 nm as the SOI layer thickness. We decided to employ the Co (Cobalt) Silicide structure since we found that it is the most stable means of reducing transistor parasitic resistance.[2] Figure 2 illustrates the transistor sub-threshold characteristics. This figure illustrates the characteristics of complete depletion type SOI transistors when both P and N type MOS transistors have a threshold voltage of 0.25 V, and the S value becomes 70 mV/dec. Photograph 1 shows a transistor cross-section.

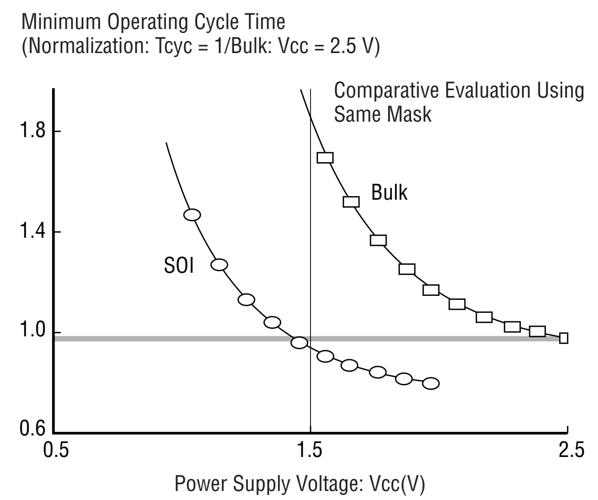
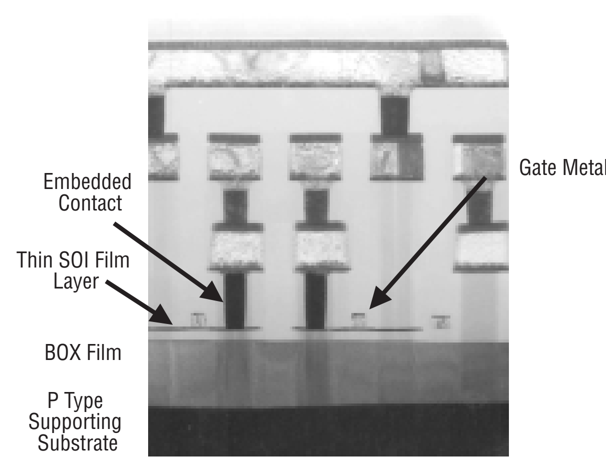


Figure 3: Power Supply Voltage Dependency of Minimum Processor Operating Cycle Time

In this photograph, it is possible to confirm that the SOI layer is very thin by using the gate metal as a comparison. We developed the advanced fabrication technology and process technology that makes this possible.

Expansion into Digital Devices

We will verify the fundamental characteristics that would result if we use this transistor in a digital CMOS device. Figure 3 compares the power supply voltage dependency of the minimum operating cycle time for a processor manufactured using this process with that of an equivalent device. Compared to bulk CMOS devices, SOI-CMOS devices can have reduced power supply voltage while maintaining operating performance, and can greatly reduce power consumption. The reduction of junction capacitance in SOI structure transistors prominently appears as a performance comparison. We have already developed low power consump-



Photograph 1: Cross-section Photograph

	Bulk CMOS	SOI CMOS Transistor	
	Transistor	Partial Depletion Type	Complete Depletion Type
S Value (mV/dec)	80 to 90	80 to 90	60 to 70
Junction Capacitance (Relative Value)	1	0.1 to 1	0.1
Parasitic Thyrister Structure	Yes	No	No

Table 1: Transistor Performance Comparison

tion 256 kb SRAM using the above characteristics and will expand it as mixed logic components.

Expansion into High-frequency Devices

Using the advantages of reduced junction capacitance and completely isolated structure, we are studying how to apply and expand into high-frequency devices used in communication LSIs. Next, we would like to discuss SOI-CMOS device performance as an RF (Radio Frequency) circuit component that is required to operate at high frequencies. Figure 4 illustrates a fundamental RF circuit block. The SPDT (Single Pole Double Throw) switch functions to separate transmission from reception and is required to reduce signal transmission loss as much as possible. Figure 5 illustrates the frequency dependency of the SPDT switch transfer coefficient in SOI/bulk MOS transistors. Since the junction capacity is small with SOI, it is possible to minimize signal transmission loss even in high-frequency areas. Also, in the case of RF circuits, many passive devices such as inductors and capacitors are used for impedance matching and frequency selection. There is much signal loss with normal Si substrates due to the high conductivity. The Q value of passive devices manufactured on this substrate decreases. Figure 6 illustrates the Q value frequency dependency when a spiral inductor is manufactured on a Si substrate with a different resistance via an equivalent insulating film. It has been confirmed that a high Q value can be obtained in the high-frequency area for inductors manufactured on high-resistance substrates. High-resistance substrates cannot be used with bulk CMOS devices since effects such as reduced latch-up tolerance would result. On the other hand, since SOI-CMOS devices employ a complete isolation structure, it is possible to use a high-resistance substrate as the supporting substrate. It is also possible to combine passive devices that have superior high-frequency characteristics.

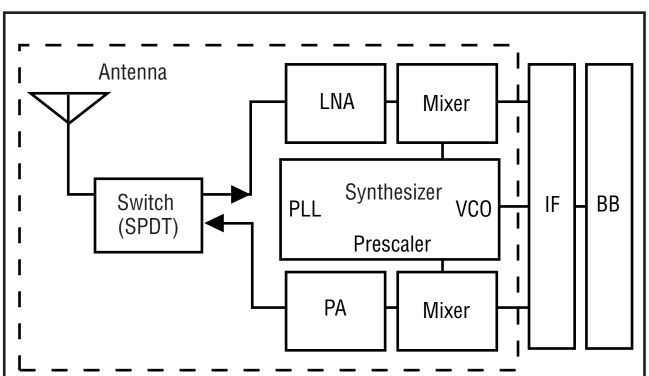


Figure 4: Simplified RF Circuit Block Diagram

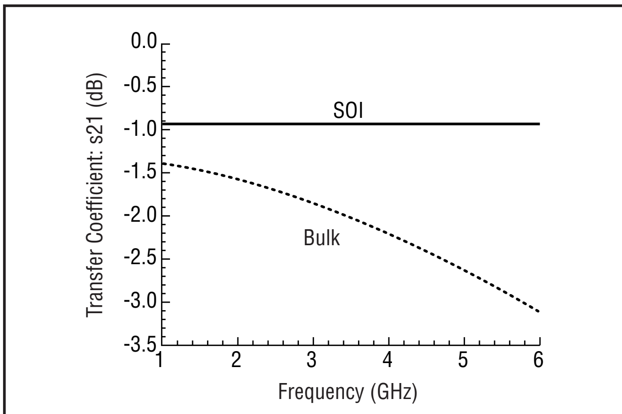


Figure 5: Frequency Dependency of SPDT Switch Transfer Coefficient

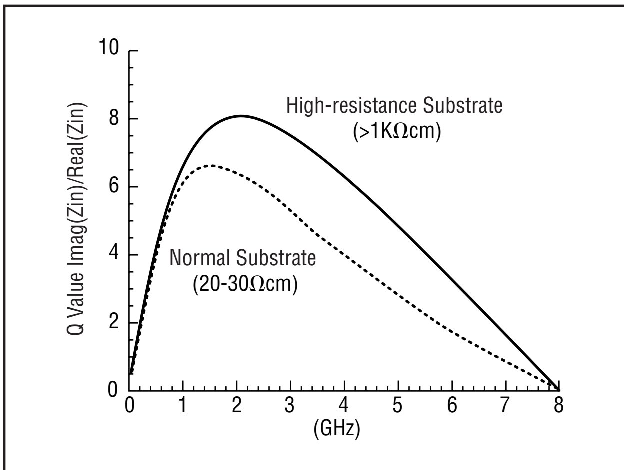


Figure 6: Q Value Frequency Dependency with Spiral Inductor

Improving Functional Quality/Reliability

When combining analog operation RF and IF (Intermediate Frequency) circuits with digital operation BB (Base Band) circuits and developing a one-chip radio transceiver LSI, then reducing cross-talk passing through the substrate becomes a major functional quality issue. Figure 7 compares the cross-talk index and frequency dependency of transfer coefficient S21 between SOI-CMOS devices using a high-resistance substrate and bulk CMOS devices. Since SOI-CMOS devices are completely separated from the substrate, combining with high-resistance substrate greatly improves the cross-talk characteristics over that of bulk CMOS devices. If this cross-talk characteristic is used, then it will be possible to develop digital-analog mixed LSI for radio transceivers that can handle GHz band high-frequency operation by employing SOI.

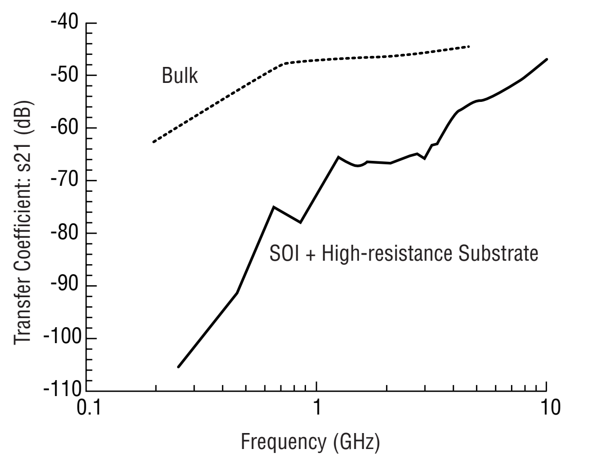


Figure 7: Frequency Dependency of Cross-talk Characteristics

Also, when reducing power consumption, operation error caused by either disturbance noise or internally generated noise resulting when the power supply voltage is decreased becomes a major reliability concern. The CMOS device latch-up phenomenon is a representative example of this.

Since the well area electrically isolates bulk CMOS devices from the substrate, a parasitic thyrister is inevitably constructed between the power supply and GND pins. Latch-up is the phenomenon in which this parasitic thyrister is activated by well/substrate current resulting from either a disturbance surge or internal transistor operation. As a result, the system will either malfunction or shut down. (See Figure 8.) This phenomenon is more likely to occur when the device integration is improved and when the device temperature increases. Placing fixed substrate layers and independent well drain holes between all devices with different polarities generally prevents occurrences of this phenomenon. However, these measures cannot prevent the area that the devices occupy from increasing. In the case of SOI-CMOS devices, each element is completely isolated by BOX oxide film and LOCOS oxide film, so no parasitic thyristers are formed and the latch-up phenomenon does not occur. It is not necessary to place fixed layers and drain layers. Also, improved integration and improved high-temperature operation performance can be expected.

Overcoming SOI-CMOS Issues

In this article we discussed the advantages of the 0.2 μm SOI-CMOS devices that were developed, but there were also issues that we needed to overcome. As is evident in Photograph 1, the SOI structure transistor is made up of a very thin SOI layer. Therefore, the SOI elements themselves can be easily thermally destroyed by electrostatic surge current from a charged human body (HBM: Human Body Model).[3]

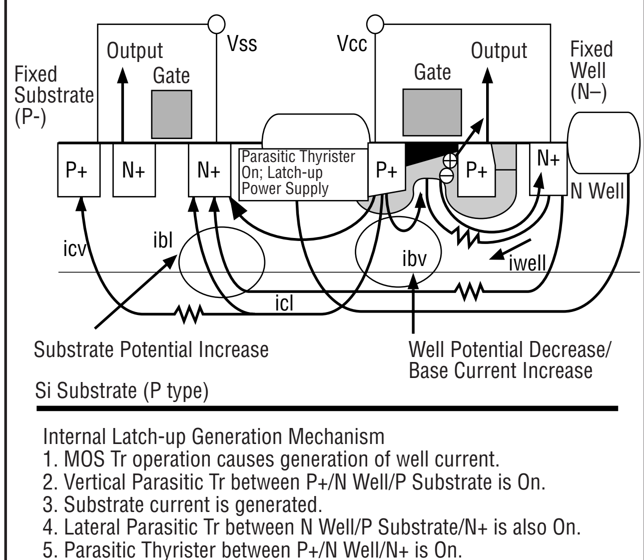


Figure 8: Explanation of Bulk CMOS Device Internal Latch-up Phenomenon

We at Oki are considering incorporating devices such as an ESD protective device into our transistor structure. We have developed protective circuitry that takes electrostatic surge response into account, so we have also realized various ESD tolerances that are appropriate for the I/O characteristics of each product.

Conclusion

In order to reduce power consumption, the power supply voltage used will probably continue to decrease and there will probably be stronger demand for devices with high-frequency operating performance. If the power supply voltage is reduced, then either soft errors caused by injecting radiation or latch-up operation error caused by disturbance noise may become quite problematic. In order to resolve these issues, we will use SOI-CMOS device technology to provide low power consumption system LSI products for analog-digital RF mixed circuits in the mobile and personal communication markets.

References

1. “Reduced LSI Power Consumption to 1/3 of Previous Level Using SOI Technology”, Fumio Ichikawa, Nikkei Electronics, March 8, 1999 (No. 738).
2. T. Ichimori, N. Hirashita, and J. Kanamori, “Advanced Co Salicide Technology For Sub-0.20μm FD-SOI Devices”, IC-SSDM, (JSAP, Sendai, 2000).
3. “Electrostatic Damage Phenomenon of Semiconductor Devices”, Yasuhiro Fukuda, Reliability Engineering Association of Japan Newsletter, Jan., 2000 (Vol. 22/No. 1).