High Frequency Bandwidth Memory Optimized for Consumer Applications

Shinzo Sakuma

Demand continues for general purpose DRAMs with a higher capacity and faster speeds to increase the performance of personal computers, which comprise the majority of DRAM applications. For this reason DRAM products on the market primarily have specifications that satisfy applications for personal computers. However, in spite of the fact that many varying aspects of specifications are required for DRAMs intended for consumer applications other than personal computers, manufacturers have no choice but to use DRAMs with specifications for personal computers. Therefore, we developed a 32 Mbit SDR SDRAM dedicated for consumer applications.

Requirements of DRAMs for consumer applications

Comparisons between specifications required of DRAMs for personal computers and those required of DRAMs for consumer applications are shown in **Table 1**. DRAMs intended for personal computers are required to have a larger capacity and faster speed. Double Data Rate (DDR) and Double Data Rate 2 (DDR2) interfaces are used to satisfy the fast speed requirement with data transfer speeds from 400 MHz to 667 MHz. Furthermore, since the assumption is that multiple chips will be used for memory modules, single package products are easily implemented with a large capacity required of individual chips, ranging from 256 Mbit to 512 Mbit. The larger capacity and faster speeds required for personal computer use, however, are not optimal for the DRAM specifications for consumer applications. Consumer application requirements are described below.

Firstly, since the surface of circuit boards is often limited for consumer applications and the single chips of DRAMs are frequently used for such purposes, SiPs, which use the Multi Chip Package (MCP) technology that involves the sealing of multiple chips in a package, are often adopted. The ease for assembling an MCP is a critical feature of the memory for this reason.

Secondly, many consumer applications involve capacity requirements that are small to medium in size. Although specific capacity requirements vary from one application to another 16 Mbit to 64 Mbit is often an adequate capacity, whereas current DRAM products with a capacity from 256 Mbit to 512 Mbit are much too large. A capacity larger than necessary is more costly, which suggests a suitably sized capacity would be more desirable.

Thirdly, applications for televisions, a growing market among consumer applications, require bandwidths between about 3 Gbit/s to 8 Gbit/s, the same as the specifications for DDR.

Table 1 Comparison of requirements for DRAMs intended for personal computers and consumer applications

	DRAMs for personal computers	DRAMs for consumer applications
Interface	DDR or DDR2	SDR or DDR
Capacity	Large capacity (256 to 512 Mbit)	Suitable capacity (16 to 64 Mbit)
Usage configuration	Externally-mounted single packages	SiP by MCP technology
Data transfer speed	400 to 667 MHz	100 to 166 MHz
Bandwidth	From 10 Gbit/s	3 to 8 Gbit/s

As mentioned above DRAMs are necessary for memory that can be assembled easily as MCPs, while incorporating suitable capacity and high frequency bandwidths for the purpose of satisfying requirements for consumer applications.

DRAM easily assembled as MCP

Pads are usually arranged on two or four sides of semiconductor chips for the purpose of connecting with packages or other chips. They are generally arranged on two sides at the edges of chips with DRAMs. An example of chips with pads on two sides, used in assembling an MCP, is shown in **Fig. 1**. Chips are often connected to the circuit board first and then connected to other chips via the circuit board as shown in **Fig. 1 (a)** or layered and connected as shown in **Fig. 1 (b)**. Concerns of the former method include an increased number of layers on the circuit board, as well as wiring resistance, capacity and quality variations, due to the fact that wiring is necessary on the circuit board. Such issues can potentially pose a major threat for triggering operational malfunctions when chips are used in high-speed operations. The circuit arrangement efficiency of the connected chip of the latter method may deteriorate since pads on the connected chips must also be distributed on two sides, thereby requiring distribution of the DRAM interface circuit on two sides as well.

Pads have been arranged on one side of the chip with this 32 Mbit SDRAM for the above reason. An example of a connection with pads arranged on a single side is shown in **Fig. 2**. **Fig. 2 (a)** depicts an example where direct connection with horizontal orientation is established with a connected chip. **Fig. 2 (b)** depicts an example of a connection with layering. In both cases consideration for the circuit board design is not

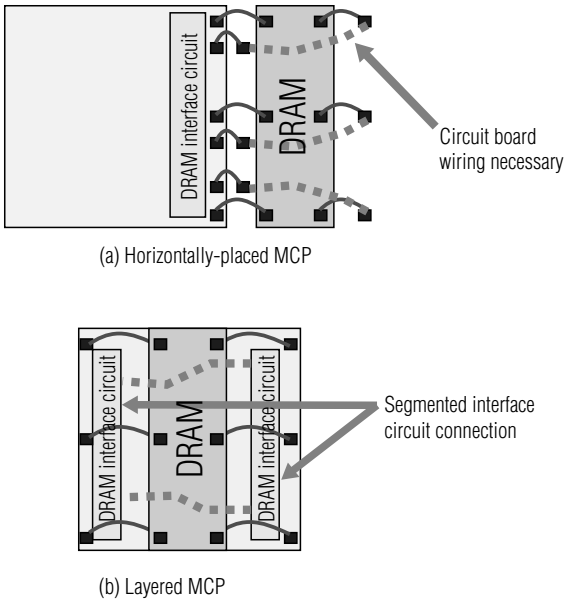

Fig. 1 Examples of MCP configurations for chips with pads on two sides

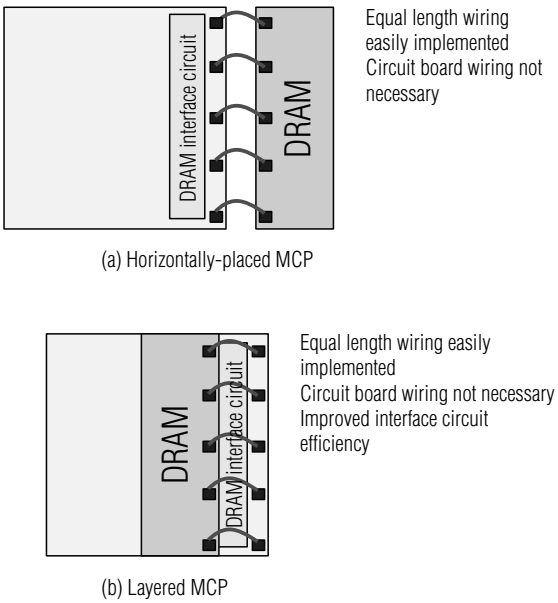

Fig. 2 Examples of MCP configurations for chips with pads on one side

necessary, as the circuit boards have no wiring. This leads to expectations regarding a reduction in circuit board costs and the risks relating to circuit boards, as well as the simplification of the circuit board design. Furthermore, quality fluctuations in the wiring can be reduced and the wiring resistance and wiring capacity minimized, since connections can be established in the shortest distance using wires of approximately the same length. Simplification of the interface for high-speed signals can be expected as a result of such effects. Furthermore, since the pads for connection can be arranged on a single side of the connected chip the DRAM interface circuit can also be concentrated on a single side, enabling other advantages, such as improved circuit arrangement efficiency.

Risks relating to circuit boards and the high-speed interface can be reduced by implementing a connection to DRAM via pads arranged on a single side, making it possible to simplify the assembly of MCP products that are often used for consumer applications, as mentioned above.

Optimum capacity selection

The capacity and bandwidth required for television applications, which are representative examples of consumer applications and for which growth is anticipated, are shown in **Fig. 2**. The memory capacity required is expressed in the following manner:
Capacity = resolution × number of gradation steps
The memory capacity required for each respective resolution is approximately 18.9 Mbit for XGA (1,024 × 768), approximately 22.1 Mbit for W-XGA (1,280 × 720), approximately 25.2 Mbit for SXGA (1,366 × 768) and approximately 50 Mbit for HDTV (1,920 × 1,080). This means that 64 Mbit is required for HDTV, whereas a capacity of 32 Mbit is sufficient for all other modes with a lesser resolution. Product lines of general purpose DRAMs have a capacity of 16 Mbit, 64 Mbit and 128 Mbit for SDR products, whereas DDR products have 256 Mbit and 512 Mbit. This means that a minimum of 64 Mbit is required for SDR products and at least 256 Mbit is required for DDR products to satisfy the requirement. DDR products have an excessive capacity for all resolutions. SDR products with a 64 Mbit capacity have an excessive capacity for all applications other than HDTV, whereas 32 Mbit products provide an optimum capacity. In the past general purpose products with a 64 Mbit capacity were available but general purpose products with a 32 Mbit capacity were not available, which made it necessary to use products with an excessive 64 Mbit capacity. We selected a memory capacity of 32 Mbit as the optimum memory capacity for single chip implementations intended for SXGA and lower modes, the most numerous for applications of low-end television sets.

Table 2 Memory capacity and bandwidth necessary for television set applications

	XGA	W-XGA	SXGA	HDTV
Resolution (kbit)	786	921	1,049	2,073
Gradation steps (bit)	24	24	24	30
Required capacity (Mbit)	18.9	22.1	25.2	50.0
Bandwidth (Gbit/s)	2.3	2.7	3.0	7.5

Optimum bandwidth

The bandwidth necessary for each respective resolution are expressed in the following manner:

Bandwidth = Resolution × Frequency × Gradation steps × 2
(frequency is tentatively calculated for 60 Hz)

Approximately 2.3 Gbit/s are required for XGA, whereas approximately 2.7 Gbit/s are necessary for W-XGA, approximately 3.0 Gbit/s for SXGA and approximately 7.5 Gbit/s for HDTV, as shown in **Table 2**. Bandwidth for each respective DRAM is shown in **Table 3**.

Assuming that bandwidth for DRAM can be obtained in the following manner:

DRAM bandwidth = number of I/Os × frequency of I/O operations × Efficiency
(efficiency tentatively calculated with 0.95)

This means that a single chip of DDR products for 16 IOs of 400 MHz (5.6 Gbit/s) is sufficient for SXGA and lower modes, whereas a single chip of SDR products for 32 IOs of 166 MHz (5.0Gbit/s) can satisfy the requirements as well. The requirement of 10 Gbit/s for HDTV can be satisfied using a single chip of DDR2 products for 16 IOs of 667 MHz (10.1 Gbit/s) or two chips of SDR products for 32 IOs of 166 MHz.

Table 3 Bandwidth for each respective DRAM

	16M SDR	32M SDR	64M SDR	256M DDR	512M DDR2
Number of IOs (bit) × 16	× 16	× 32	× 32	× 16	× 16
IO frequency (MHz)	166	166	166	400	667
Bandwidth (Gbit/s)	2.5	5.0	5.0	5.6	10.1

A comparison of characteristics for SDR and DDR, which are available options, is provided in **Table 4**. Although bandwidths for single chips are almost the same with 5.0 Gbit/s and 5.6 Gbit/s, the operating frequencies of IOs, on the other hand, are 166 MHz and 400 MHz respectively, with SDR less than half the speed of DDR. Risks relating to operational malfunctions of the system are low, since in general lower frequencies involve a lower degree of difficulty with their design.

In order to transfer data at high speeds a high-speed interface, which can accommodate operations at a high frequency, must be incorporated in connected chips with DDR, therefore, a process with a design to accommodate high speeds is necessary. In other words, because the requirements for process and high-speed performances are low for chips connected to SDRs, it is considered that costs can potentially be optimized for the overall system.

Furthermore, for the purpose of configuring MCP, operations had to be guaranteed by testing the DRAM in a wafer condition. Wafers, however, can only be tested up to 140 MHz, which is the effective maximum frequency that can be realized at the present time. Mismatching with actual speeds is less likely with SDRs therefore, the related risks are considered to be slimmer.

An SDR with specifications that include an interface with 32 IOs and a frequency of 166 MHz has been selected as DRAM that satisfies the bandwidth required for SXGA as well as lower modes and the risks are small for the system as a whole.

Table 4 Comparison of SDR and DDR

	SDR × 32	DDR × 16
Clock frequency	166 MHz	200 MHz
IO operating frequency	166 MHz	400 MHz
Minimum operating frequency	None	Approx. 83 MHz
Power supply voltage	3.3 ±0.3 V	2.5 ±0.2 V
Operating guarantee on wafer	○	△
Bandwidth	5.0 Gbit/s	5.6 Gbit/s

32 Mbit SDR SDRAM

The main specifications of the 32 Mbit SDR SDRAM we developed, which is dedicated for consumer applications, is shown in **Table 5**, whereas a photograph of the chip is shown in **Photo 1**. A capacity of 32 Mbit, suitable for television applications for SXGA and lower modes, was selected. The memory bandwidth of 5.0 Gbit/s was secured by selecting 32 bit as the number of IOs and maximum operating frequency of 166 MHz in order to satisfy the bandwidth requirement of 3.0 Gbit/s. The SDR interface was selected as it is an interface that presents a potential to have a lower risk and overall reduced costs. The ease of MCP assembly was improved by arranging pads for connection on a single side, as shown in a connection example depicted in **Photo 2**.

Table 5 Main specifications of 32 Mbit SDR SDRAM

Capacity (words × bits)	32 Mbit (1,048,576 × 32)
Pad arrangement	One side of chip
Max. operating frequency	166 MHz
Max. bandwidth	5.0 Gbit/s
Power supply voltage	3.3 ±0.3 V

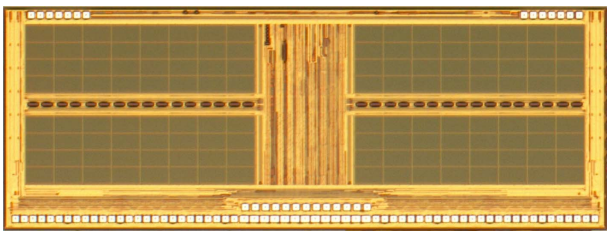

Photo 1 32 Mbit SDR SDRAM chip

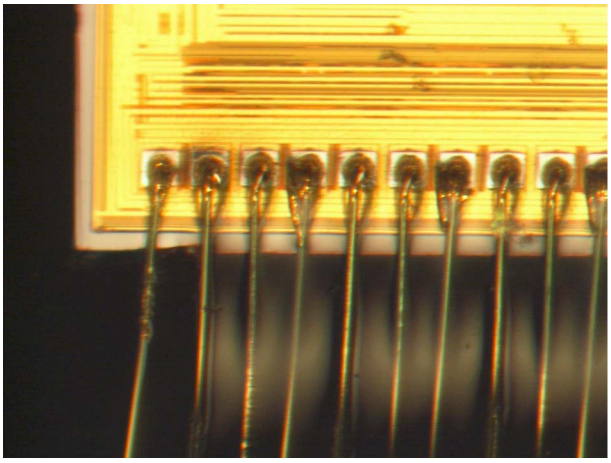

Photo 2 Example of pad wiring on a single side

Conclusion

We developed a 32 Mbit SDR SDRAM, which is a DRAM with specifications optimally suited for consumer applications and is easily implemented due to the improved ease of incorporation in MCP. We intend to continue with our developments to provide memory products that are optimally suited for functions and performances, truly necessary for our customers.

Authors

Shinzo Sakuma: Silicon Solutions Company, System Memory Business Div., ASM Design Dept.

TIPS

[Descriptions of Basic Terms] Glossary

DDR

A DRAM interface using a method that inputs and outputs data at the edge of the rise and fall of the clock.

SDR

A DRAM interface using a method that inputs and outputs data only at the edge of the rise of the clock.

SiP

A system configured by inserting an MPU or memory in a single package.

MCP

An assembly technology, which involves the insertion of multiple chips into a single package.