Low-Power LSI Technology of 0.15 µm FD- SOI

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Recently, there has been an increasing demand for portable, battery-operated devices like cellular phones. Achieving low-power, high-speed LSIs is essential to miniaturize these devices and improve performance and extend battery life. In order to meet such demands, we have applied the 0.35µm and 0.20µm Fully Depleted SOI CMOS device to LSIs, and low-power LSI technology has been developed.

This paper describes the development of the 0.15µm FD-SOI CMOS device fabricated for the purpose of miniaturization and speed improvement, and the performance of digital circuits using this device. First of all, the methods used to achieve a low-power LSI will be described. Secondly, the structure and electrical characteristics of the 0.15µm FD-SOI CMOS device with multiple threshold voltages, will be described. Finally, the experimental results of low-voltage digital circuits are described.

Low-Power design methodology

Many general methods to reduce the power of LSIs have been proposed from algorithm- level to process-level[1)] and applied to LSIs. Common standard methods that can be applied to most LSIs are lowering the supply voltage and using CMOS devices. Lowering the supply voltage is the most effective and direct way to achieve low-power LSIs because the power consumption is proportional to the square of the supply voltage. Therefore, the LSI which operates at a frequency of 100MHz at a supply voltage of 1V or less are being widely studied and developed[2) 3)].

FD-SOI CMOS is superior to conventional bulk CMOS for low-voltage operation, because the parasitic capacitance is reduced and the subthreshold characteristics of the transistor are precipitous. We developed a 0.15µm FD-SOI CMOS device with multiple threshold voltages, which made it possible to reduce the leakage current and improve speed.

Development of 0.15µm FD-SOI CMOS device

Due to the shrinkage of the gate length of the MOS device, the drivability is improved, but a short channel effect occurs, which results in the lowering of the threshold voltage. Through the increase of the channel impurity concentration to suppress this effect, a reduction in drivability will occur. This cycle is a common issue in submicron MOS devices. On the other hand, the increase of the channel impurity concentration leads to a partial depletion, which deteriorates the superiority of the FD-SOI CMOS that was described previously in this paper. In order to realize an FD-SOI CMOS device with a multiple threshold voltage, it is necessary to develop simple and stable processes with a consideration for quality and cost concerns for each threshold voltages device.

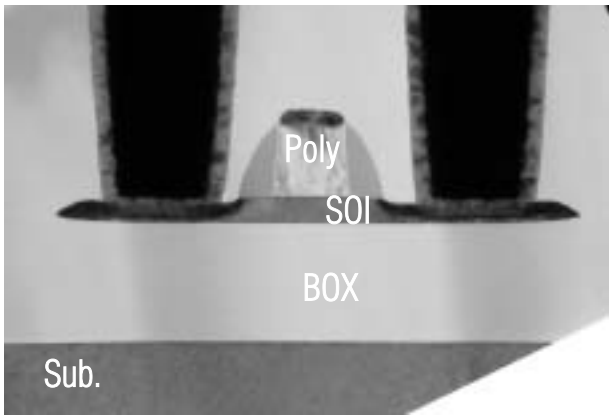

Fig. 1 Cross-sectional TEM photograph of a 0.15µm FD-SOI transistor

FD-SOI MOS transistor. Bonded SOI wafer was used. The thickness of the SOI on the buried oxide (BOX) and the thickness of the gate oxide are 40nm and 2.5nm, respectively. Since the FD-SOI CMOS is fabricated on the extremely thin SOI layers, we developed a total process, which suppresses the thinning of SOI for the source/drain region. In the 0.15µm SOI process, the backend process (BEP) is the same as the 0.16µm logic process used in our Fab., for the purpose of making effective use of our existing process technology and design kit.

(1) Thin-film SOI process technology

It is necessary to confirm the minimum thickness of the SOI layer from a viewpoint of the reduction of the diffusion layer resistance by applying the self-aligned silicide (salicide) technology to thin-film SOI devices. Figure 2 shows the dependence of a Co silicide sheet resistance on the width of the patterned N+ diffusion layer with a various thickness of SOI (t_{soi}).

t_{SOI} is defined as the thickness of the SOI layer under the gate electrode. The SOI film for the source/drain region is thinner than that for the channel. In the case of this 4 nm thick Co, the sheet resistance for various patterned width are low enough when the SOI thickness is thicker than 30nm. On the other hand, the sheet resistance increases on 25nm thick SOI. This increase of sheet resistance is explained by the remaining CoSi after

the 2nd RTA, due to a lack of Si for the transition from CoSi to $CoSi_2$.

In the Co salicide process, there was the other issue of BOX leakage failure, which occurred because of an electrical short between the SOI and substrate due to a pinhole made by over-etching at the contact opening. This issue was improved by the optimization of a contact hole etching process and the adoption of the Contact Hole Etching Prior to the Second Annealing (CHEPSA), in which the contact-hole etching is performed prior to the 2nd RTA for the transition form CoSi to $CoSi_2$. Figure 3 shows the distribution of the BOX leakage current. If the current determines the failure over 1x10-11A, it is indicated that the BOX yield will be improved from 20% to 100% by using CHEPSA. From the TEM image of figure 1, it is confirmed that a 25nm thick cobalt silicide is formed over the diffusion layer and the gate and that the contact hole etching is stopped above the silicide layer.

(2) Optimization of transistors

In order to suppress the short channel effect, we used a pocket ion implantation, which is used for bulk devices and increases the substrate impurity concentration only near the gate edge. As shown in Figure 4, the threshold voltage roll-off is improved by the pocket ion implantation. Although the variation of the threshold voltage for the fluctuation of 0.02μm gate length was maximally 270mV, without the pocket ion implantation, it dramatically decreases to approximately 30mV with the pocket ion implantation. The short channel effect was sufficiently suppressed in both the NMOS and PMOS.

In order to increase the driving current, the S/D extension structure is introduced instead of the LDD structure, which is used in 0.20μm FD-SOI CMOS devices. This structure achieves the higher impurity concentration with a shallow junction between the channel and the source/drain region. As a result, the parasitic resistance was decreased, which made it possible to obtain an increase in the driving current by about 15%, thereby making acceleration of the device processing speed possible.

The I-V characteristics of each transistor are shown in Figure 5.

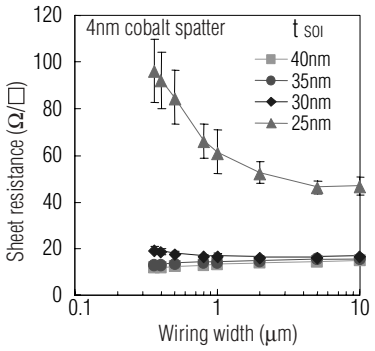

Fig. 2 The dependence of a Co silicide sheet resistance on the width of patterned N+ diffusion layer with various thickness of SOI

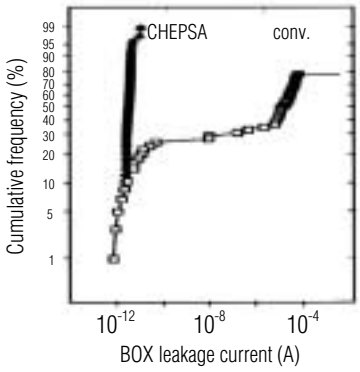

Fig. 3 Cobalt salicide process comparison of the distribution of the BOX leakage current

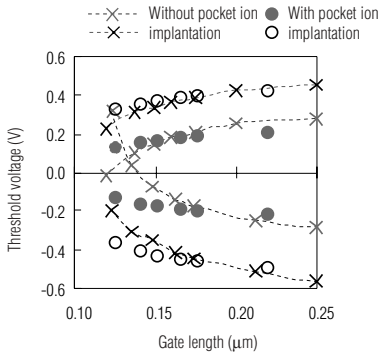

Fig. 4 The dependence of the threshold voltage on the gate length and effect of the pocket ion implantation (S/D extension structure transistors)

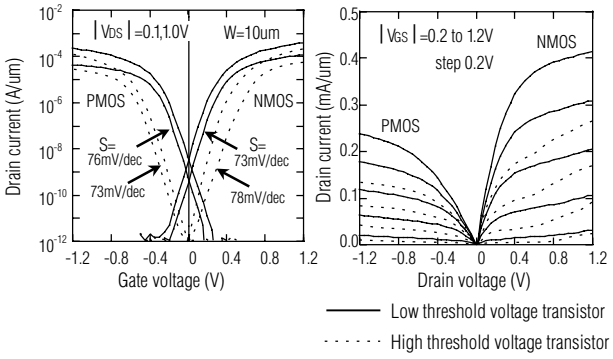

Fig. 5 I-V characteristics of 0.15μm FD-SOI-CMOS

The subthreshold factor is approximately 75mV/dec for all transistors. This value is adequately smaller than that of bulk CMOS or partially-depleted SOI CMOS in the same generation (about 85mV/dec or higher). It is confirmed that this 0.15μm SOI device shows fully-depleted characteristics. The kink characteristics[5] appear in high threshold voltage NMOS transistors. The reason is considered to be the substrate floating effect due to holes, which are generated by the hot carriers effect.

Low-voltage digital circuits

We verified the performance of digital circuits using 0.15μm FD-SOI CMOS. The circuits include a 32-bit adder circuit, 64Kb SRAMs, and a 16-bit DSP core that uses these functional blocks.

(1) 32-bit adder

In order to evaluate the performance of the fundamental arithmetic circuit, we fabricated a 32-bit adder using a binary carry look ahead architecture[6]. The architecture can improve the speed of the adder with a long bit length such as 32-bit because the carry of each bit is generated from the propagate and the generate signals with a binary tree. Further, it is suitable for the adder with a long bit length because the speed is proportional to the logarithm ($\log_2$) of the bit length.

Figure 6 shows measured delay time and power consumption of the 32-bit adder. The delay time of 1.9ns and the power consumption of 1.9μW/MHz were obtained at a supply voltage of 1V. Further, the minimum operating voltage was confirmed to be 0.4V.

(2) 64Kb SRAM

For the purpose of comparison an SRAM configured with a low threshold transistor, an SRAM configured with a high threshold transistor, and an SRAM configured with MT-CMOS[1], were contained on the test chip.

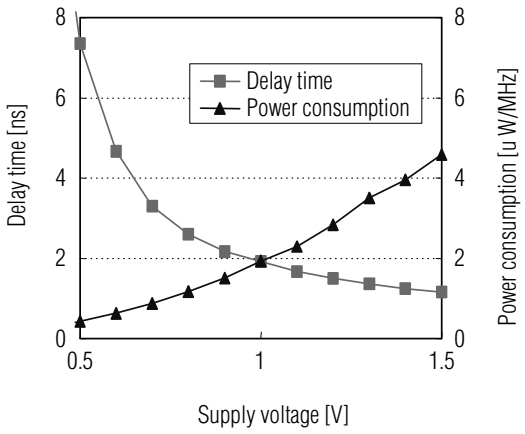

Fig. 6 Measured delay time and power consumption of the 32-bit adder versus supply voltage

The features of the MT-CMOS configuration is that low threshold transistors are used in the peripheral circuit and high threshold transistors in the memory cell. The peripheral circuit is connected to the power source via the power switch with high threshold transistors. Since the memory cell needs to preserve data while in the standby mode, it is connected directly to a power supply line.

Figures 7 and 8 show measured clock access time and standby leakage current of the 64Kb SRAM respectively. The clock access time of the MT-CMOS configuration is 2.9ns at a supply voltage of 1V. A speed improvement of approximately 50% was obtained as compared with the SRAM configured with high threshold transistors that is 5.3ns. Further, the standby leakage current of the MT-CMOS configuration is 2.6μA. It is a reduction by about 1/1000 lower than the SRAM configured with low threshold transistors that are 0.9mA. From these results, we confirmed the effectiveness of the MT-CMOS configuration that can achieve high-speed and low standby leakage current.

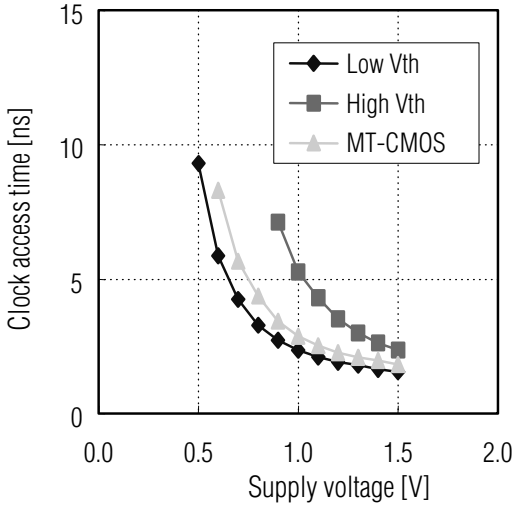

Fig. 7 Measured clock access time of the 64Kb SRAM with various transistor configurations versus supply voltage

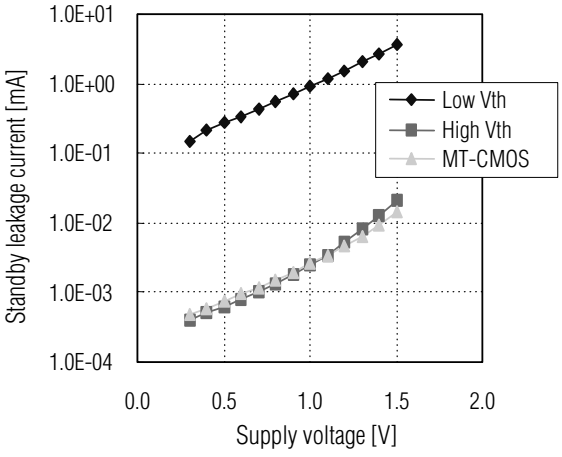

Fig. 8 Measured standby leakage current of the 64Kb SRAM with various transistor configurations versus supply voltage

(3) 16-bit DSP core

Further, we fabricated the 16-bit DSP core using these functional blocks. As shown in Figure 9, the 16-bit DSP core is configured by the 256Kb (64Kb x 4) data memory, data pointer, and the multiplier accumulator, which consists of a 16-bit multiplier circuit and a 32-bit adder circuit. It reads two sets of 16-bit data from the data memory, and executes a calculation of the sum of products with the multiplier accumulator.

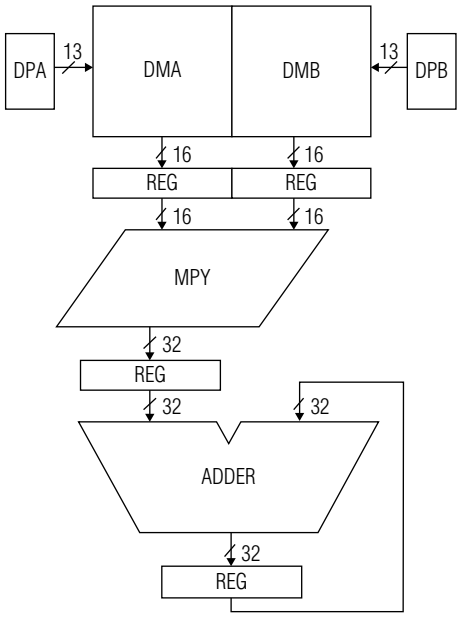

Fig. 9 Block diagram of the 16-bit DSP core

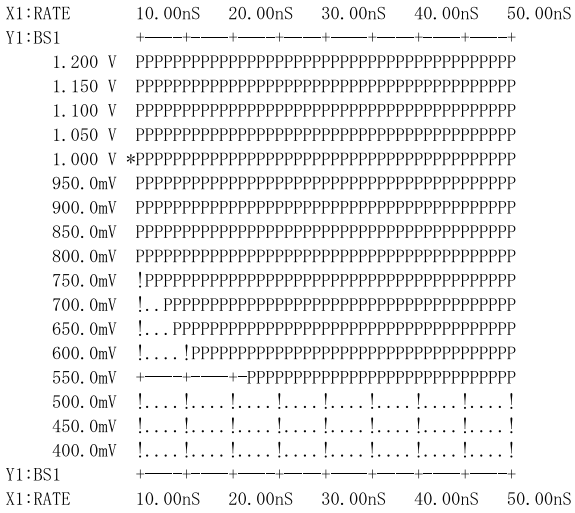

Fig. 10 SHMOO plotting of the 16-bit DSP core

Measurement plotting (SHMOO plotting) of the operable range for the power voltage and clock cycle time is shown in Figure 10. The 16-bit DSP core was fabricated using a 0.15μm FD-SOI CMOS device. An operating frequency of 100MHz and a power consumption of 9mW were obtained at a supply voltage of 0.8V.

Conclusion

This paper described the development of the 0.15μm FD-SOI CMOS device with multiple threshold voltages and the experimental results of low-voltage digital circuits. We confirmed the operation of the 32-bit adder, down to 0.4V, and achieved a power consumption of 9mW (@100MHz/0.8V) with a 16-bit DSP core, and verified that FD-SOI CMOS is effective for low-power operation. In the future, we intend to develop the analog circuit and the RF circuit etc and evolve these efforts into a low-power system LSI by utilizing the characteristics of the FD-SOI, which is effective for low-voltage operation.

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