Development of the NR-FIFO Series Imaging Noise Reduction LSI

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The NR-FIFO (Noise Reduction-FIFO) series imaging noise reduction LSI, with its low cost superior noise reduction capability, was developed in response to the high image quality requirements of liquid crystal television sets, plasma displays, and other AV products. It was developed by integrating the noise reduction circuitry for image signals and the memory for storing image data on a single chip through the use of the DRAM-LOGIC consolidation process. The ML87V2104 is an LSI with an I/P conversion function that has, besides the noise reduction function a double-speed conversion function, while the ML87V2013 is an LSI with an I/P conversion function.

Purpose for the NR- FIFO series development

Television sets and flat panel displays have increased in popularity in recent years, while screen sizes have become larger very rapidly. Due to this, the effects of image signal noise that was not noticeable previously in smaller screens, has become more noticeable. In order to improve the image's quality, noise reduction technology has become essential.

Conventional noise reduction functions were the source of high costs because they were configured with external memory. In order to raise the image quality and reduce costs we invented an LSI that provides both a noise reduction function and a memory on a single chip.

FIFO[*1)], installed in imaging related equipment, is called the “field memory” or “frame memory”, and is used as the data stack memory for image processing because memory management is easier with FIFO than with the universal DRAM. FIFO was adopted as the memory for storing image data for the NR-FIFO series because the ease in using its memory management was brought to our attention.

Further, it was possible to merge far more high quality image functions with the NR-FIFO, such as double-speed conversions, interlacing, and progressive conversions (I/P conversion), by loading consolidated FIFO macro that incorporates optimal functions and configurations for applications.

It is possible to obtain image signals with the noise removed, and without making any major changes to the current system of the user, simply by inserting this NR-FIFO we developed, onto the image signal line.

Noise reduction function

Firstly, the noise reduction function that is loaded into the ML87V2104 and the ML87V2103 will be described.

There are numerous and varying types of image noise, ranging from ghosts that are often seen on television screens, to block noise that is generated during the compression and decompression of data, such as MPEG. The type of noise the NR-FIFO is intended to process is mainly random noise that is generated in regions that have a weak electric field and areas with poor radio wave conditions. In order to reduce this random noise, the field-recursive noise subtraction-type three-dimensional noise reduction method, which we developed, was adopted for the ML87V2104 and the ML87V2103. Images with reduced noise can be obtained by first extrapolating the level of noise based on the difference between two consecutive images (the current input field data and data which is just one field prior to it), and then by subtracting this from the current input field data.

When this kind of two-dimensional image data is handled along a time axis, such as the present and the past, it is called a three-dimensional noise reduction. To make this happen it is necessary to read the past field data while storing the current field data, and this can be easily achieved by using a FIFO macro that has two ports, one for reading and one for writing, which can be operated asynchronously. Configuration of the noise reduction segment is shown in Figure 1.

The performance of the noise reduction function depends on whether pure noise components can be extracted from the difference in values between the fields. In the case of still image input, for example, the difference in value, between two identical locations on two images, can be determined entirely as noise components.

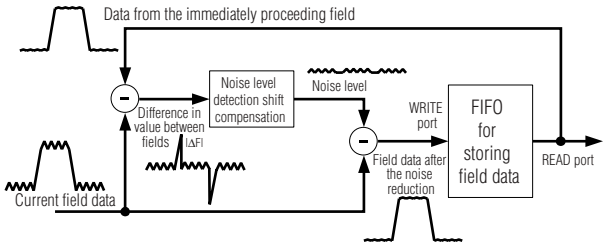


Fig. 1 Configuration of the noise reduction segment

*1) FIFO is an abbreviation for First-In First-Out. It is a function that writes data in the same order as it is read. This is a basic function that is loaded into the field memories, which are referred to as FIFO.

Interlaced signals skip lines when scanning images, therefore, two consecutive field data will exist with a different structure, one of an even line field and one of an odd line field. For this reason, the position of an image being compared will shift with the field-recursive noise subtraction method, which results in this component becoming the difference in value between the fields. Further, if a motion picture is input, the “motion” component of the image will be included in the difference in value of the fields. Therefore, it is necessary to distinguish between “motion” and "noise" from the difference in values. The following methods are used with the NR-FIFO series, in order to estimate the noise levels from the difference in the values between fields:

1. Insertion of a noise level detection filter.
2. Prediction of motion from data of a neighboring horizontal picture element.

Figure 2 shows the method for detecting the level of noise using the noise level detection filter. A noise detection region is set by multiple parameters, and the sides of the noise detection region are used as functions for detecting noise, to determine the specific level of detected noise from the difference in value between fields. Further, it is possible to adjust the noise detection level by changing parameter settings. When the difference in value between fields is small, this filter will distinguish it as “noise”, although if it is large, it will be determined to be “motion”.

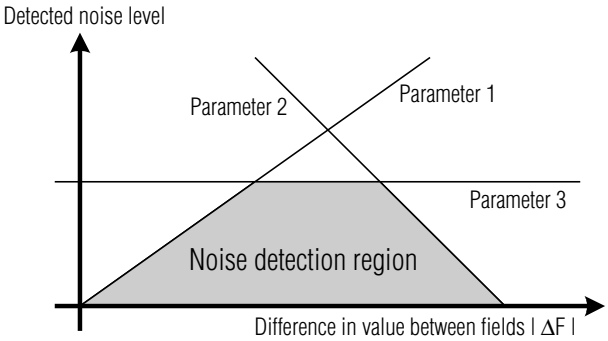


Fig. 2 Noise level detection filter

Further, a reduction in the erroneous detection of noise components and its effect is being sought by compensating the current field data input for motion, when “motion” is predicted in the image with the prediction function using a neighboring horizontal picture element data.

Effects of noise reduction

Image signals loaded with random noise, were created by reducing the image signal input levels. The signal was then transmitted, and input into the NR-FIFO, to evaluate the noise reduction effects.

Results of the evaluation indicate that the random noise levels that were seen as slight movements on the screen were reduced to approximately one-third. The improvement effect was verified to be about 10dB in terms of its signal-to-noise ratio. Photo1 demonstrates the effects of noise reduction, with the left half of the screen showing an image that has had no noise reduction, whereas the right half shows an image that has had the noise reduction process applied.

Phot. 1 Noise reduction effects

More sophisticated functions and lower costs

A noise reduction function is not the only incorporated benefit. There are also high image quality functions, such as a double-speed conversion function for the ML87V2104 and an I/P conversion of the ML87V2103 that was made possible with the NR-FIFO. Descriptions of more sophisticated functions and cost reductions are provided below, based on the actual development of these LSIs.

It was possible for the ML87V2104 to reach the standards of high image quality required by the two television broadcasting standards(NTSC and PAL)[1)], because of its noise reduction function, as well as its double-speed conversion function. The specification summary of the ML87V2104 is shown in Table 1.

Double-speed conversion is a technology used to inhibit the flickering (flicker) of screen images, which occurs in displays with low frame rate formats, such as the PAL standard that is predominantly used in the European region.

Table. 1 Specification summary of the ML87V2104

Power voltage	3.3V ± 0.3V
Internal memory	4.4MB (960 x 288 x 16-bit) x1
Maximum input operating frequency (demultiplex/multiplex)	18MHz/36MHz
Input image signal	525/60Hz, 2:1 625/50Hz, 2:1
Input format	16-bit YCbCr, 4:2:2 8-bit YCbCr, 4:2:2 ITU-R BT.656
Noise reduction function	Field-recursive noise subtraction-type three-dimensional noise reduction (3D-NR)
Maximum output operating frequency (standard speed/double-speed conversion)	18MHz/36MHz
Output image signal	525/60Hz, 2:1 525/120Hz , 2:1 625/50Hz, 2:1 625/100Hz, 2:1
Output format	16-bit YCbCr, 4:2:2
Package	100-pin QFP

These functions are made available through the use of a FIFO macro that has two ports, a write port and a read port, which can independently operate asynchronously. Firstly, a FIFO macro is necessary to configure the field-recursive operating segment of the noise reduction function. In order to perform a double-speed conversion, it must be possible to read, at double the speed, the FIFO macro read operation frequency of the noise reduction segment, which means another FIFO macro is necessary. Further, by connecting these in a cascaded manner, both the noise reduction function and the double-speed conversion function can be made available (Figure 3).

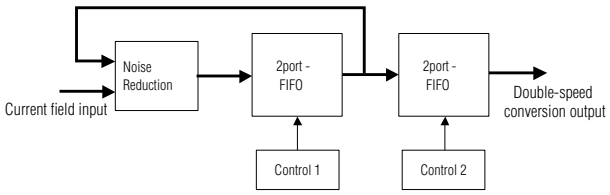


Fig. 3 Example of a configuration with conventional technology (1)

If two FIFO macros with two ports are loaded, the chip size will increase. In order to prevent this, we decided to develop a three-port FIFO macro by adding a read port, capable of an asynchronous operation, to the two-port FIFO macro, and then loading this to the ML87V2104. The three-port FIFO macro has a larger area than the two-port FIFO macro, due to an increase in the number of read register and control circuits. However, in the overall picture of the chip, this is a reduction in chip area to 58.9% of the area used by two sets of two-port FIFO macros, although it is maintaining the same performance.

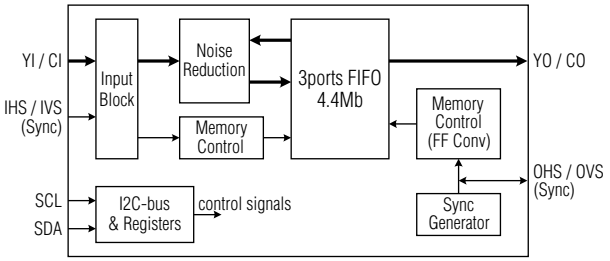


Fig. 4 Block diagram of the ML87V2104

With the ML87V2104, we succeeded in developing a low-cost, single chip LSI that offers noise reduction and double-speed conversion functions by loading this three-port FIFO macro. The block diagram of the ML87V2104 that we developed is shown in Figure 4.

Next, the sophisticated functions and lower cost of the ML87V2103 will be described. The ML87V2103 is an LSI that not only provides a noise reduction function, but also an I/P conversion function for flat panel display outputs, as well. A specification summary of the ML87V2103 is shown in Table 2.

Table. 2 Specification summary of ML87V2103

Power voltage	3.3V ± 0.3V
Internal memory	3.9MB (768 x 320 x 16-bit) x1
Maximum input operating frequency (demultiplex/multiplex)	14.75MHz/29.5MHz
Input image signal	525/60Hz, 2:1 625/50Hz, 2:1
Input format	16-bit YCbCr, 4:2:2 8-bit YCbCr, 4:2:2 ITU-R BT.656
Noise reduction function	Field-recursive noise subtraction-type three-dimensional noise reduction (3D-NR)
Maximum output operating frequency (standard speed/IP conversion)	14.75MHz/29.5MHz
Output image signal	525/60Hz, 2:1 525/60Hz , 1:1 525/120Hz, 2:1 625/50Hz, 2:1 625/50Hz, 1:1 625/100Hz, 2:1
Output format	16-bit YCbCr, 4:2:2
Package	100-pin QFP

I/P conversion is a technology that takes interlaced signals, derived from image scanning every other line, and converts them into successive scan (progressive) signals by creating line data of the skipped segments. The ML87V2103 determines the existence of a correlation between the image data by using four lines of data. Further, a line data that does not exist in a real field is created through the use of a single line data from a previous field, for the purpose of providing an I/P conversion function with a high image quality. If these existing macro memories were used to configure the LSI, a two-port macro would be needed in the field-recursive segment of the noise reduction function, as well as a two-port FIFO macro (for storing past field data) and four line memory macros (for reading four consecutive line data simultaneously), as shown in Figure 5.

If the FIFO and line memory macros are used to configure the LSI, as shown in Figure 5, there will be an increase in the size of the chip, along with an increase in the electric current consumption. For this reason, we developed a seven-port FIFO macro with five ports, capable of simultaneous readings as well as two ports for reading and writing, which form the noise reduction field-recursive segment.

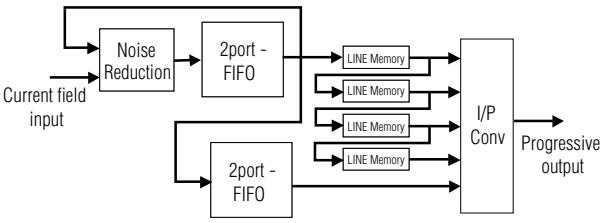


Fig. 5 Example of a configuration with conventional technology (2)

Of these five new ports, four of them are to make it possible to read four consecutive line data, while the last port is intended for reading the previous field data. Further, a special function for internal transmissions was

implemented for the purpose of reading past field data. This is a function that transfers the previous field data, which was stored at the same address as the current field data that is destined for storage, to a stack region, before storing the current field data in the FIFO. All these made it possible to realize functions with a single macro that previously required two FIFO macros and four line memory macros. Therefore, it was possible to load the ML87V2103 with both the noise reduction function, as well as an I/P conversion function, through the loading of this seven-port FIFO macro. Further, the area of the chip is limited to 56.7%, which results in a lower cost when compared with existing FIFO and line memory macros. A block diagram for the ML87V2103 is shown in Figure 6. Further, Photo 2 shows a photograph of the ML87V2103 chip.

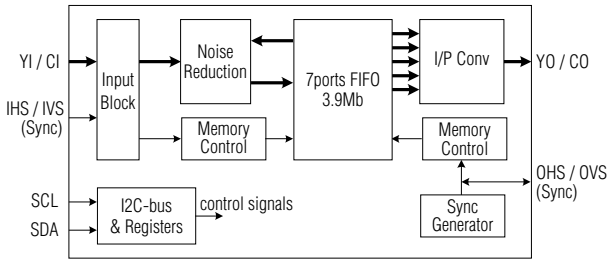
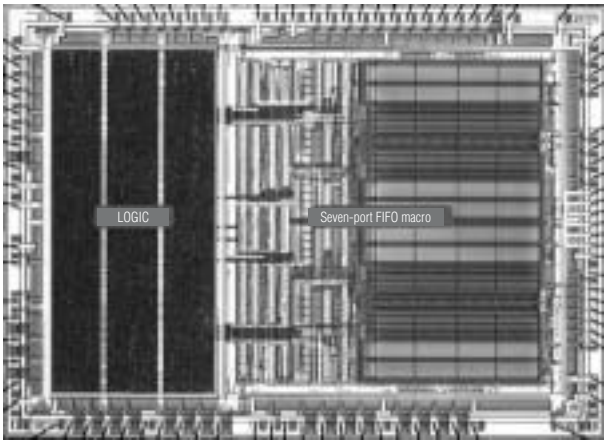


Fig. 6 Block diagram of the ML87V2103



Phot. 2 Photograph of the ML87V2103 chip

As described above, in developing the NR-FIFO series products, we customized the FIFO macros into forms that made it possible to easily provide functions and performances required by the market, while keeping the chip size small and its power consumption low. By combining this with the logic, it was possible to create high value added products. Further, with the noise reduction function we developed, it became possible to distinguish between the image “noise” and “motion”, making it possible to reduce the random noise on the image signal to a level where it is hardly visible even on a large screen. Using these technologies, it was possible to realize products that respond to the higher image quality and lower cost demands of the AV product market.

Postscript

Image noise reduction LSIs of the NR-FIFO series were developed using the DRAM-LOGIC consolidation process and the FIFO customization technology, which offers superior noise reduction capabilities, with lower costs.

Further, we intend to complete the NR-FIFO series product lineup, with more sophisticated functions, in pursuit of an even higher image quality, and for a much lower cost. This will be achieved through the improvement of a process technology that will bring about miniaturization, the development of high image quality algorithms, as well as development of FIFO macros that are optimally suited for algorithms.

References

1) Transistor Technology Special, CQ Publications, No. 52, 2001.

Authors

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