# CMOS-RF transceiver LSI for Bluetooth<sup>TM</sup>

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Bluetooth<sup>™\*1)</sup> is one of the global standards for short-distance wireless communications. By permitting two-way radio connections between a number of electronic devices, such as portable phones, PCs, printers, digital cameras, audio players, etc., it allows sound files, images, and data to be exchanged between these devices. The frequency of Bluetooth™ is in the Industry Science Medical Band, 2.4 - 2.5 GHz, which can be used without a radio licence, and the related communications standards have been published by the industry group, Bluetooth SIG (Bluetooth Special Interest Group). Hence, this wireless communications system has the potential for worldwide implantation, and is widely anticipated to replace cable connections for everyday devices in the home, office, car, and elsewhere, in the future,

Table 1 shows the main specifications for Bluetooth<sup>™</sup> radio communications. In order to guarantee mutual connectability of radio communications, the Bluetooth SIG has set up its own independent certification system. On 6th September 2001, Oki Electric's radio-frequency (RF) transceiver LSI (ML7050LA) obtained official certification for the latest Bluetooth<sup>™</sup> standard <sup>2)</sup> from the certification body <sup>3,4)</sup>. The special features of this LSI are that it provides Bluetooth™ RF transceiver functions via a single chip by CMOS processing, whilst also reducing the number of external components. By connecting an antenna, a 2.4 GHz band pass filter, and resistors as well as capacitors to this LSI, it is possible to transmit and receive radio signals in the 2.4 GHz waveband.

Table 1	Bluetooth v.1.1	RF specifications <sup>2)</sup>

Radio Frequency	2.4 GHz - 2.4835 GHz
Channel spacing	1 MHz
Transmission power	0.25 mW - 2.5 mW
Modulation method	Frequency hopping spectrum
	dispersion
Primary modulation method	Gaussian-filtered frequency shift
	keying (GFSK)
Frequency hopping	1600 / sec
Modulation index	0.28 - 0.35
Data rate	1 Mbps
Sensitivity level	0.1 nW (-70 dBm)
Maximum usable level	10 μW (-20 dBm)

Moreover, by connecting our baseband LSI (ML70511LA), it is possible to construct a short-distance wireless network based on the Bluetooth<sup>TM</sup> standards.

In this article, we shall look at the general composition of the RF transceiver LSI (ML7050LA), and the composition of the transmitter and receiver.

#### Overview of RF transceiver LSI (ML7050LA)

Fig. 1 schematically shows the composition of the RF transceiver LSI. This LSI comprises the functions

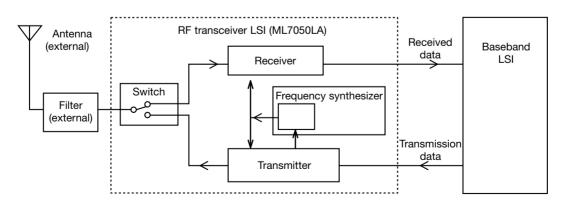


Fig. 1 Overview of RF transceiver LSI (ML7050LA) (omitting reference frequency signal and control signals, etc.)

\*1) "Bluetooth" is a trademark of Bluetooth SIG, Inc. USA

of: (1) receiving 1 Mbps digital data from the baseband LSI and placing the data on a 2.4 GHz radio wave for transmission; and (2) extracting data from a received radio wave, restoring it to a digital signal, and transferring this signal to the baseband LSI.

We start with a brief description of how the transmitter operates. There are 79 Bluetooth™ channel frequencies in total, spaced at 1 MHz intervals between 2402 and 2480 MHz. In general, when Bluetooth<sup>™</sup> is used to connect a pair of transceivers together, the transmitter and receiver are operated alternately at intervals of 625 µsec, during which the transmission/ reception frequency may also hop to other channels. This occurs because the 2.4 GHz band is used to exchange radio waves for various different applications, and therefore hopping is performed in order to guarantee a connection via another channel if one channel becomes congestion. and also in order to increase communications privacy. The transmission frequency is determined by the oscillation frequency of the frequency synthesizer. Each time frequency hopping is performed, the synthesizer receives an oscillation frequency command from the baseband LSI and starts oscillating at the designated channel frequency. The transmitter mounts digital data received from the baseband LSI onto the transmission wave generated by the frequency synthesizer, by means of a frequency modulation method, and sends this as a radio wave via the antenna.

By means of the filter, the receiver detects a 2.4 GHz band signal, from the various radio frequencies arriving at the antenna. The 2.4 GHz band may contain radio signals from another Bluetooth<sup>™</sup> device, as well as non-Bluetooth<sup>™</sup> signals. The receiver circuit selects the signals of the desired channel frequency by means of the super-heterodyne method (which converts the frequency of the wanted signal to an intermediate frequency (IF)), and then extracts the data carried on the received wave. The intermediate frequency of this LSI is 2 MHz.

In Bluetooth<sup>™</sup>, it is possible to assign one wireless

Table 2 Specifications of transmitter	
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Waveform shaping filter		
Circuit type	Gm-C low pass filter	
Frequency synthesizer (for transmitter & receiver)		
External input clock	11, 12, 13 MHz	
Phase comparator frequency	1 MHz	
Power amplifier		
Circuit system	AB class	
Output power	1.6 mW (2dBm)	

device as a master device, and up to 7 other wireless devices as slaves. Communications among the master device and the slaves are based on repeated transmit and receive operations. In other words, none of the wireless devices transmits and receives at the same time. Therefore, it is sufficient to provide just one frequency synthesizer in the RF transceiver LSI, as illustrated in Fig. 1. This simplifies the circuit design and reduces the cost of the LSI, resulting in a very wide range of application. Below, the internal block of the transmitter and receiver will be described.

#### Block structure of transmitter and receiver

Fig. 2 shows the block structure of the transmitter of this LSI.<sup>5)</sup> Broadly divided, the transmitter circuit consists of a waveform shaping filter, a frequency synthesizer, and a power amplifier. Table 2 summarizes the specifications of this transmitter circuit.

The waveform shaping filter excludes highfrequency harmonics in the digital waveform, from the transmission data signal (1 Mbps, digital) received from the baseband LSI. The filtered data signal has sub-1MHz components and an analogue signal waveform.

The frequency synthesizer comprises a VCO (Voltage Controlled Oscillator) and a PLL (Phase Locked Loop). The phase comparator of the PLL in this LSI operates at 1 MHz. The division ratio of the

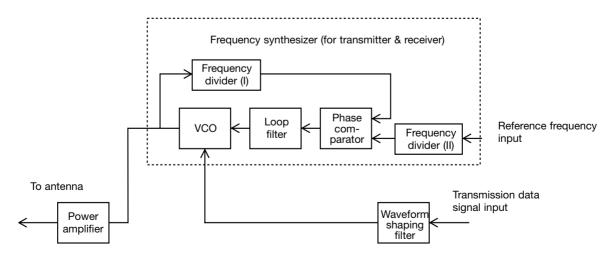


Fig. 2 Block diagram of transmitter

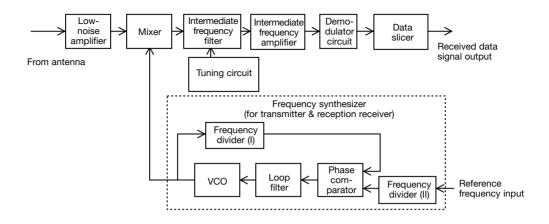


Fig. 3 Block diagram of receiver

frequency divider (I) is set by the baseband LSI each time the frequency hops, and the required frequency oscillation output is obtained by feeding back the divided frequency to the phase comparator.

The data signal passed by the wave shaping filter is input to the frequency modulation terminal of the VCO, and this causes the capacitance of the resonance circuit (comprising a parallel inductor and capacitor) to change directly. This gives rise to modulation in the frequency of the transmitted wave of +/- 150 kHz with respect to the channel frequency. The transmission signal carrying the data is then amplified by the power amplifier, to an output power of 1.0 - 2.5 mW (0 - +4 dBm) at the output terminal of the LSI. This power is attenuated by approximately 40% (2 dB) by the external filter (see Fig. 1), yielding an output of 0.6 - 1.6 mW (-2 - +2 dBm) at the antenna end.

Fig. 3 is a block diagram of the receiver. The specifications of this circuit are given in Table 3. The power of the received signal is amplified by a factor of 25 at a low-noise amplifier. Generally, the signal-to-noise ratio on the receiver side is dictated to a large degree by the noise figure and power gain of the front-end amplifier<sup>6</sup>. In the design stage, we have sought to minimize the noise figure in the 2.4 GHz spectrum, whilst optimising the power gain, by incorporating the floating components of the LSI package, bonding wires, and the like, into our simulations. The mixer combines the amplified signal with the signal from the frequency synthesizer, and converts the carrier frequency from the 2.4 GHz band to an intermediate frequency of 2.0 MHz.

In addition to the target IF frequency (2 MHz), the output from the mixer contains the signals  $2\pm1$ , 2, ... MHz located in the adjacent channels. These interference waves are removed by the IF filter. A tuning circuit is used to fix the intermediate frequency and avoid the effects of product variations in the filter elements, or change in the ambient temperature. The

IF signal is amplified by 40dB at the intermediate frequency amplifier, and then demodulated by the demodulator. An analogue waveform comprising data at a rate of 1 Mbps will be superimposed on the DC voltage component of the demodulated signal.

A data slicer extracts the DC voltage component of the demodulated wave, and converts the parts of the analog signal with a voltage higher than the DC voltage to a High CMOS level, and the signal parts with a lower voltage to a Low CMOS level, thereby converting the received data into a digital signal.

#### Table 3. Specifications of receiver

Low-noise amplifier			
Power gain	14 dB		
Noise figure	5 dB		
Input-referred third-order intercept point	-12 dB		
Mixer			
Power gain	21 dB		
Noise figure	25 dB		
Image rejection ratio	32 dB		
Intermediate frequency	2 MHz		
Intermediate frequency filter			
Circuit type	Gm-C band pass filter		
Tuning method	Automatic tuning by PLL		
Filter pass band	2 MHz +/- 500 kHz		
Intermediate frequency amplifier circuit			
Circuit type	Differential limiting amplifier		
Voltage gain	40 dB max.		
Demodulator circuit			
Circuit type	Delay detection system		

For compatibility with Bluetooth<sup>™</sup> frequency hopping, the data slicer requires a function which can detect the DC voltage component of the demodulated signal very quickly. Each time that the other transceiver starts to send data, the data slicer in the present LSI is able to detect the DC voltage level accurately from the demodulated signal waveform, within a period of several µsec from the start of transmission.

### Development of high-frequency circuits

A 0.35µm CMOS process is used in the manufacture of this LSI chip. In designing high-frequency radio circuits, low-loss inductors and capacitors are vital for impedance matching. We completed an inductor library using conventional process. As for capacitors, we reduced their parasitic capacitances and electrode resistances by building metal/insulator/metal capacitors.

High-frequency circuit design also demands a clear understanding of the parasitic components of each element. S parameters of inductors, capacitors, transistors, pads, bonding wires, and the package were measured up to10 GHz, and equivalent circuits containing their respective parasitic components were built to further enhance design accuracy.

## Oki's Bluetooth<sup>™</sup> solution

Fig. 4 shows a photograph of our module combining the RF transceiver LSI (ML7050LA) and the baseband LSI (ML70511LA). This module is controlled by Host Control Interface (HCI) to provide data connection between modules. In portable devices, office modules, or the like, radio communications with other Bluetooth<sup>™</sup>-enabled devices can be made by supplying connection commands and data to the module in accordance with HCI. Oki has designed a System Development Kit (SDK) to aid the development of upper-layer HCI software. This means that with the Oki module and SDK, our customers are able to build short-distance wireless networks based on Bluetooth<sup>™</sup>, and develop the software required to operate these networks.

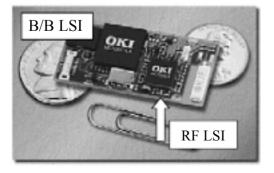


Fig. 4 RF transceiver LSI (ML7050LA : indicated by arrow) incorporated in module. The LSI on the left-hand side is the baseband (B/B) LSI (ML70511LA).

#### Conclusion

The LSI presented here (ML7050LA) is based almost wholly on analog circuitry. In general, replacing analog circuits with digital circuits not only enables minimum design size for transistors, but also permits reduction in power consumption and footprint. Next-generation RF transceiver LSIs will have digitalized IF (intermediate frequency) signal processor circuits and minimum transistor processing dimensions reduced to 0.18  $\mu$ m from 0.35  $\mu$ m currently. These advances will reduce power consumption and minimize the footprint of the chip. We can also expect to see enhanced functionality, with the introduction of baseband functions, and the like.

## References

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