

System LSIs for third-generation mobile communications terminals

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On 1st October 2001, NTT DoCoMo started the world's first full-scale W-CDMA (Wideband Code Division Multiple Access) service, under the title FOMA ("Freedom of Mobile multimedia Access"). W-CDMA, as a system, was established by the International Standard IMT-2000 (International Mobile Telecommunications – 2000) to provide high-speed, high-quality multimedia services, such as voice, data and animated images, in mobile environments.

By enabling high-volume data transmission, which permits swift retrieval of information anywhere in the world, W-CDMA has given rise to a wide variety of mobile communications terminals, alongside conventional voice terminals, such as PDAs or other data terminals, and vehicle-mounted terminals; (these devices are commonly known as "third-generation mobile communications terminals".)

In wireless setups, WLANs (Wireless Local Area Network) and PANs (Personal Area Network) are attracting particular attention due to the easy connectability they provide, by linking individual terminals with their peripherals by radio links.

In this field, Oki is looking to enable seamless connections between public subscriber networks based on W-CDMA, and peripheral networks, or PANs, belonging to individual users. In other words, we are aiming to develop system LSI products which achieve "seamless public network to PAN connection", in order to offer baseband system solutions.

This essay looks at baseband system solutions, the characteristics of baseband signal processing, and the particular features of related system LSIs.

Baseband system solutions

Offering a baseband system solution means providing:

- (1) system LSIs which realize "seamless public network to PAN connections"
- (2) communications software
- (3) evaluation boards.

The following products are used in our baseband system solution :

- Control LSI (ML7101)
- Baseband signal processor LSI (ML7102)

- AFE (Analog Front End) LSI (ML7081)
- W-CDMA protocol stack (software)
- Baseband signal processor control (software)
- Evaluation board

Control LSI (ML7101)

This LSI comprises our basic platform, the μ PLAT[®]-92 core based on the ARM920T[™] CPU, plus a TeakLite[™] DSP, and is fitted with Bluetooth, USB and high-speed UART as its main peripheral functions.

Baseband signal processor LSI (ML7102)

An LSI containing a baseband signal processor compliant with Release 99 of the 3GPP (3rd Generation Partnership Project)¹⁾, the technology standards body for W-CDMA systems.

AFE-LSI (ML7081)

The ML7081 LSI is mounted with an 8-bit reception A/D converter, 10-bit transmission D/A converter, and a generic 8-bit A/D converter.

W-CDMA protocol stack

This software runs on the real-time OS, μ ITORN, and implements the protocols required for connection to a base station.

Baseband signal processor control

This software provides control of the ML7102 and the radio section, as well as interfacing with upper-layer protocols.

Evaluation board

The evaluation board consists of a radio section, baseband section, and man/machine interface section, and incorporates the basic functions of a mobile communications terminal. Software development assistance interfaces are provided by JTAG and ETM9 for the μ PLAT[®]-92, and JTAG for TeakLite[™]. Peripheral interfaces for Bluetooth, USB devices and UART are also fitted.

System LSIs for installation in third-generation mobile communications terminals must satisfy high-performance specifications, and the software they use to provide communications, applications and other services is very complex.

Therefore, alongside our system LSIs, we also supply protocol stack software and baseband signal processing control software for W-CDMA communications, to help the customer in developing this complicated software.

This solution does not incorporate a radio device, so one must be fitted in order to evaluate the unit as a third-generation mobile communications terminal.

One of our initiatives has been to provide an evaluation board containing the basic features of a mobile communications terminal, to facilitate the evaluation of the baseband signal processor, and development of application software.

By providing the three key features (1) to (3) described above in a baseband system solution, the peripheral networks of individual users can be connected freely to public networks based on W-CDMA.

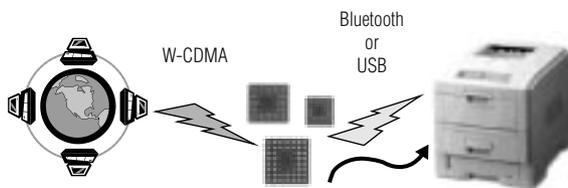


Fig. 1 Baseband System Solution (Example)

Fig. 1 shows one example of a baseband system solution using Oki products. Our system LSIs and software enable products which can, for example, download music recordings whilst simultaneously downloading and printing the related cover art and photographs. If the user does not have a printer at home, then he or she can use one in a convenience store, or elsewhere. This is the kind of service that third-generation mobile communications terminals can provide.

Characteristics of baseband signal processing

Baseband signal processing is the key technology in the system LSIs which form the basis of third-generation mobile communications terminals. The principal characteristics of baseband signal processing are described below.

- High-speed packet transmission
Uplink : 384 kb/s
Downlink : 384 kb/s (MC = 1 ~ 3)
- Transmission Diversity : Compatibility with:
SSDT (Site Selection Diversity Transmission)
STTD (Space Time Transmit Diversity)
TSTD (Time Switched Transmit Diversity)
Closed Loop Mode 1.2
- Power control
pen/Close compatibility
- Hand-off

Inter and Intra frequency (Compressed mode A, B) compatibility

The baseband signal processor must be reduced to the minimum possible LSI power consumption, due to the mobile environment. In the ML7012 (baseband signal processor LSI), we investigated the potential power savings at system level and device level. In seeking to suppress system level power consumption, we focused in particular on the sampling rate of the ML7081 (AFE-LSI) which samples the data input to the ML7012. In general, lowering the sampling rate means reduced power consumption, but the sampling rate for transmission/reception data also governs the performance of the baseband signal processor. Therefore, it must be confirmed beforehand that the unit meets the performance standards set by 3GPP. We carried out simulations to compare and verify performance in the ML7081, using sampling rates of two times and four times the chip rate (3.84 MHz), (Chip x 2) and (Chip x 4). These confirmed that the desired performance can be achieved by inserting an interpolation filter.

Table 1 shows sample timing conditions. (1) in Table 1 shows a standard BER (Bit Error Rate) comparison, at 8 times the chip rate (Chip x 8). (2) in Table 1 indicates the conditions adopted by Oki, in other words, a case where an interpolation filter is inserted at a Chip x 2 sampling rate in the ML7081. (3) and (4) show cases without an interpolation filter, at Chip x 4 and Chip x 2, respectively.

Fig. 2 gives the simulation results for BER characteristics in the four conditions in Table 1. As Fig. 2 shows, case (2), the option selected by Oki, is closest to the performance of the reference case (1). Moreover, the E_b/N_0 (Energy per bit to noise power density ratio) required for a BER of 10^{-3} is some 0.4 dB less than case (3).

In this way, we have devised a method for not only cutting power consumption by reducing the sampling rate of the ML7081 to Chip x 2, but also maintaining performance by inserting an interpolation filter.

Furthermore, power savings at device level have been made, by raising the transistor threshold to reduce the leak current, and by switching the clock on and off in function units.

In this way, we at Oki have looked into power savings at system level and device level in providing our baseband system solution.

Features of system LSIs

Fig. 3 is a block diagram of a third-generation mobile communications terminal using an Oki system LSI.

As shown in Fig. 3, the ML7101 has interfaces with the Oki products, ML7041, ML2857, ML7050 (bottom right-hand block). The ML7101 uses the μ PLAT[®] platform which combines high operating speed and low power consumption.

Table 2-1 to Table 2-3 show the features of three different LSIs.

By supplying these chipsets and the software described above, we enable easy development of

Table 1 Sample timing conditions

	Sampling rate	Sample timing shift	Interpolation filter
①	x 8	none	no
②	x 2	1/4chip	yes
③	x 4	1/8chip	no
④	x 2	1/4chip	no

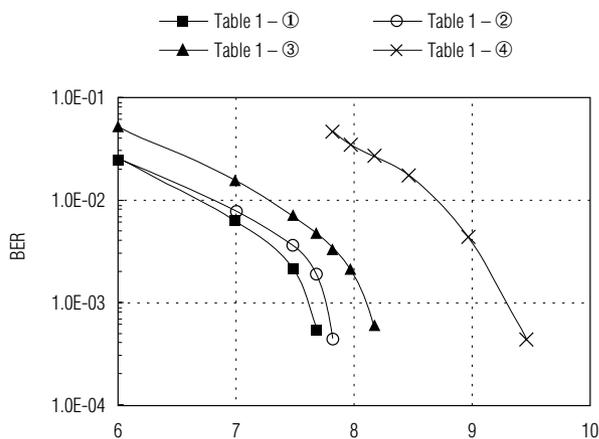


Fig. 2 BER characteristics according to sampling correction

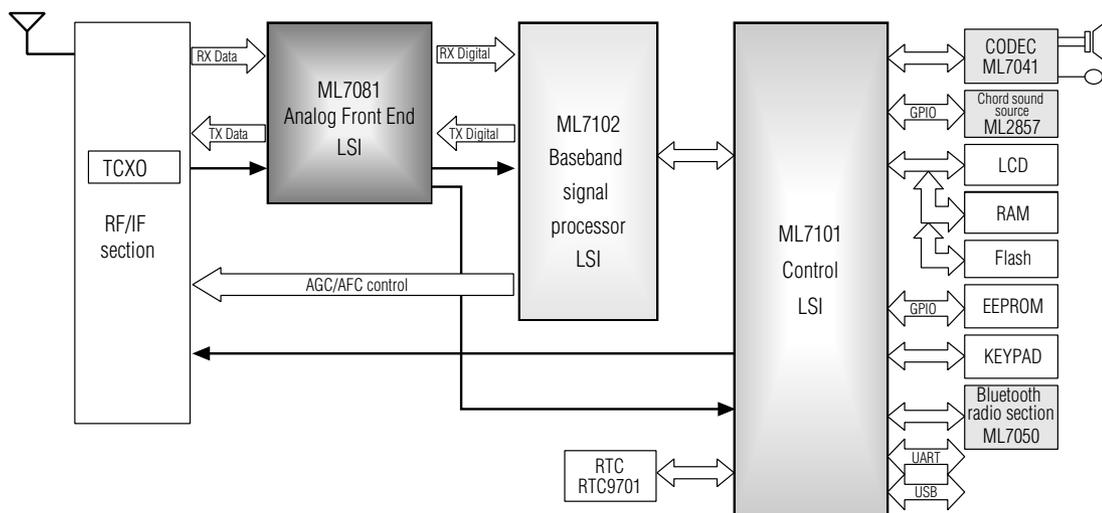


Fig. 3 Block diagram of third-generation mobile communications terminal equipped with Oki system LSIs

baseband sections for third-generation mobile communications terminals as illustrated in Fig. 3.

Our company has also developed an evaluation board comprising the basic functions of a mobile communications terminal. This board set combines a radio section, baseband section, and man/machine interface section, and by using this board, the customer is able to concentrate his efforts on application development.

The ML7101 is currently under trial manufacture as an in-house evaluation chip, which is tested on the evaluation board (Photo 1). Moreover, the ML7102 and ML7081 completed trial manufacture in February this year and are scheduled for system evaluation as chipsets.

Conclusion

We have looked here at Oki's baseband system solution, which provides system LSIs for third-generation mobile communications terminals.

This solution comprises a chipset containing a control LSI (ML7101), a baseband signal processor LSI (ML7102), and an AFE-LSI (ML7081), as well as a W-CDMA protocol stack, baseband signal processor control software, and an evaluation board. This paper has given an outline of the solution and its various specifications.

In our future schedule, we plan to continue system evaluation, in order to be able to provide solutions of high added value.

Table 2-1 Specifications of ML7101

Model Name	Main specifications
ML7101	<p>μPLAT[®]-92 :</p> <ul style="list-style-type: none"> • ARM920T™ • Data cache 16 kB • Command cache 16kB <p>DSP module :</p> <ul style="list-style-type: none"> • TeakLite™ • Program RAM RAM 60kW x 16 bit • Data RAM(X/Y) 32kW x 16 bit • Shared RAM 1kW x 32 bit <p>Peripheral interfaces :</p> <ul style="list-style-type: none"> • Bluetooth (Ver. 1.1) baseband • USB device (Ver. 1.1) • GPIO (48 ch : CPU control; 8 ch : DSP control) • High-speed UART (2 ch, max. 921.6 kb/s, of which 1 ch shares pins with GPIO) • SIO (1 ch) • KASUMI (F8, F9) <p>Clocks :</p> <ul style="list-style-type: none"> • External input 10 – 24 MHz • CPU 5/6/7/8 multiplier • DSP 3.3/4/4.7/5.3 multiplier • Bluetooth/USB/UART external input 12 MHz • Real Time 32.768 kHz <p>Package :</p> <ul style="list-style-type: none"> • 336 pin FBGA (17mm x 17mm) <p>Power supply voltage :</p> <ul style="list-style-type: none"> • Core section 1.8V • I/O section 1.8/2.5/3.3V <p>Technology :</p> <ul style="list-style-type: none"> • 0.18μm CMOS

Table 2-2 Specifications of ML7102

Model Name	Main specifications
ML7102	<p>W-CDMA baseband signal processor section :</p> <ul style="list-style-type: none"> • Band limiting filter (transmission/reception) • Synch complement / follow • Modulation/demodulation • Channel encoder (including Turbo encoder) • Channel decoder (including Turbo, Viterbi decoder) • Reception automatic gain control circuit x 2 • Transmission automatic gain control circuit x 2 • Automatic frequency control <p>Other :</p> <ul style="list-style-type: none"> • Sleep timer <p>Package :</p> <ul style="list-style-type: none"> • 224 pin FBGA (13mm x 13mm) <p>Power supply voltage :</p> <ul style="list-style-type: none"> • Core section 1.8V • I/O section 1.8/2.5/3.3V <p>Technology :</p> <ul style="list-style-type: none"> • 0.18μm CMOS

References

1) 3GPP (3rd Generation Partnership Project) HP
<http://www.3gpp.org/>

Table 2-3 Specifications of ML7081

Model Name	Main specifications
ML7081	<p>Filter :</p> <ul style="list-style-type: none"> • Baseband low-pass filter built in <p>Reception ADC :</p> <ul style="list-style-type: none"> • I and Q 2 ch. 8 bit <p>Transmission ADC :</p> <ul style="list-style-type: none"> • I and Q 2 ch. 10 bit <p>Generic ADC :</p> <ul style="list-style-type: none"> • 4 ch. selectable 8 bit <p>Input clock :</p> <ul style="list-style-type: none"> • 19.2MHz/14.4MHz selectable <p>Package :</p> <ul style="list-style-type: none"> • 84 pin BGA (7mm x 7mm) <p>Power supply voltage :</p> <ul style="list-style-type: none"> • 3.0V <p>Technology :</p> <ul style="list-style-type: none"> • 0.35μm Mixed-signal CMOS

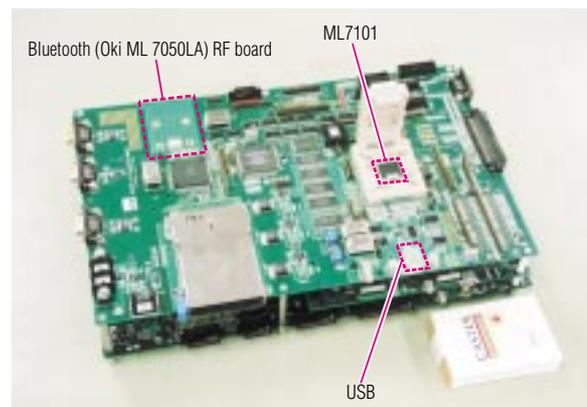


Photo. 1 Control platform evaluation board

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