Evaluation by LSI Process Diagnostics for Systems Requiring High Degree of Reliability

Kazuhiro Yabe Daiki Tanaka Katufumi Noda Sadao Suganuma
Katsumi Oka Satoshi Kuboyama Sumio Matsuda

The prerequisite for aerospace parts and components used for spacecraft systems is a guaranteed high degree of reliability, however, supply of aerospace parts and components has become a difficult task, which makes the technology an important issue for selecting and converting these items from among parts and components for household use.

Even outside the space industry, the failure of electronic devices required to have a high degree of reliability, such as those related to aeronautical, automotive, electrical and communication lifelines can not only result in large losses but may also become a problem that can cause a negative effect on the lives of people. For this reason, the selection of electronic devices that have a high degree of reliability is a big issue for users of LSI devices for such systems.

Evaluations of electronic devices with reliability tests require an immense amount of time and a lot of samples, aside from the fact that the selection of present day electronic devices with improved reliability in reliability tests conducted under general conditions are, for the purpose of practical implementation, a near impossibility. Further, since reliability tests under extreme conditions involve the wear and tear of an electronic device, there is a need for a new method for selecting electronic devices for systems that require a high degree of reliability.

A conventional evaluation of an electronic device involved the implementation of reliability tests in parallel with a conforming article analysis to complete a comprehensive quality evaluation[1),2)]. The concept of the conforming article analysis is based on the Destructive Physical Analysis (DPA) of the MIL standards (US military standards) and can be considered as an analysis method with a proven reliability. This method, however, is intended to primarily seek out defects and non-conforming structures arising from problems in the assembly process. Further, even though we have seen intensive progress made in this field in recent years, the standards have not been updated. For wafer processes even the latest standards apply only to design rules that are equivalent in a scale of tens of micrometers and are no longer appropriate evaluation methods for the latest LSIs for which progress has been made in terms of micro-structuring and multi-layering.

Consequently, we decided to have a fresh look at the wafer process of the LSI and develop an "LSI process diagnosis system" that evaluates the reliability of electronic device processes based on the existence or lack of structural abnormalities and inherent defects arising from non-conformity in the wafer process. The system is applied to a selection of electronic devices for evaluation intended for use in systems required to have a high degree of reliability[3)].

LSI process diagnosis system

We consider the LSI process diagnosis system to be a promising means for selecting from among present day electronic devices with improved reliability, as it observes in detail the internal structure of electronic devices, which are electrically conforming articles, to determine the existence or lack of defective elements inside the electronic device that can in the future become a source of failure and it speculates on the risks of failure arising from variations in structure.

The LSI process diagnosis system we developed is intended for use on a selection of electronic devices with five inspection items for the purpose of evaluating the wafer processing conditions as well as conducting a diagnosis and a rating that uses the obtained data, through a comparison with 54 evaluation items and their diagnosis standards. Further, a database system that makes it possible to diagnose, manage and operate a large volume of data obtained through inspections is also available.

(1) Inspection items of LSI process diagnosis

The five inspection items of the LSI process diagnosis are shown in Table 1. Although each individual inspection item is a part of an analysis menu for conforming articles in general, inspection conditions and inspection points are defined for each inspection item for the purpose of evaluating electronic device processes. Since the process diagnosis involves inspections of a fine structure,

Table 1 Five inspection items for process diagnosis.

No.	Inspection item	Observation equipment	Subject of inspection	Detected causes for failure
1	Surface observation	OM	Passivation Metallization	Discoloration, cracking, voiding and existence of foreign materials, etc.
2	PV film removal observation	SEM	Metallization (top)	Causative factors for voids, foreign materials and mask structural failures (wiring widths, wiring pitch, gate sizes, etc.)
3	Etch back observation	OM/SEM	Interlayer dielectric film Metallization	
4	Cross-sectional SEM observation	SEM	Layering structure Wiring, gate electrodes, contacts, etc.	Coverage structural factors for voids, foreign materials(film thickness, gate lengths, contact radius, etc.)
5	Cross-sectional TEM observation	TEM	Layering structure and composition Oxidized gate film, contacts, etc.	Structural factors for voids, foreign materials, transformations (thickness of oxidized gate film, etc.)

there is the possibility that different results may be obtained if, for example, the sampling methods of the inspection conditions differ. Defining inspection conditions and inspection points are crucial for conducting a quantitative diagnosis.

Although the setting of these conditions relies heavily on accumulated know-how regarding failure analysis and structural analysis conducted in the past, determinations are also being made on approximately 100 types of additional electronic devices through a trial process diagnosis. These inspection conditions vary greatly, mainly according to the design rules set for the electronic devices, however, at the present time it is possible to accommodate electronic devices with a design rule of up to 0.18 micrometers.

(2) Analysis procedure for LSI process diagnosis

The analysis procedure for an LSI process diagnosis is conducted according to the analysis procedures described in Figure 1, to make it possible to conduct the appropriate inspections even for electronic devices for which the layering structures or design rules are not known.

The preliminary cross-sectional investigation and preliminary etch back inspection, conducted to obtain circuit information, should be mentioned as features of the inspection procedure. Conditions, such as the layering structures and film thickness, are acquired through a preliminary cross-sectional investigation, while based on this information the preliminary etch back investigation is conducted to obtain etch back conditions and to extract circuit block information inside the chip.

Many electronic devices are composed of numerous circuit blocks and it is normal for them to have varying gate lengths and minimum wiring widths for each block. Stipulating proper analysis procedures, including preliminary investigations, is crucial for conducting reliable inspections on circuit cross-sections of the smallest structural component, since ordinarily the weak point in the wafer process is the circuitry, which is the smallest structural component configured according to the value of the design rule

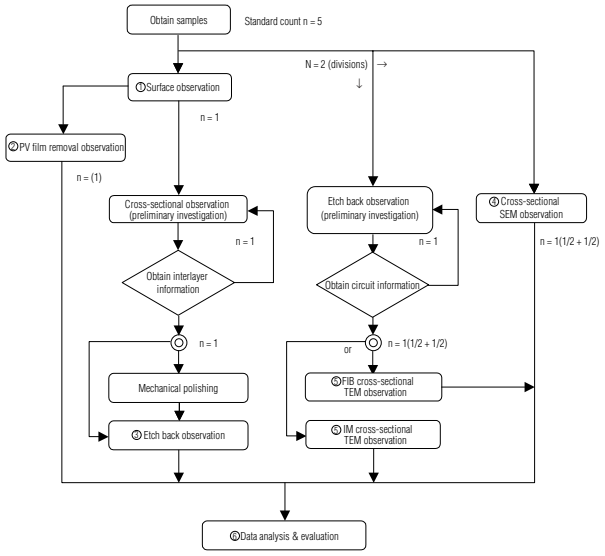

Fig. 1 Inspection procedures for LSI process diagnosis.

TIPS Basic Glossary

[Description of Abbreviations]

MIL standard: US military standards
OM: Optical microscope
SEM: Scanning electron microscope
TEM: Transmission electron microscope

Table 2 Evaluation items for process diagnosis (partial listing).

Defect item No.	Process name	Defect item	Defect item No.	Process name	Defect item
1	Wafer	Crystallization defects, pin holes, cracks and slips	21	Electrodes and wiring formation I	Voids and scratches
2	Wafer	Deformities and etching defects (bird's beak)	22	Electrodes and wiring formation I	Interfusion of foreign materials and contamination
3	Wafer	Interfusion of foreign materials	23	Electrodes and wiring formation I	Over-etching (interlayer dielectric films)
4	Wafer	Dispersion abnormalities and alignment defects	24	Electrodes and wiring formation II	Coverage of connecting sections (tapered connections)
5	Gate formation (oxidized films)	Genuine defects, crystallization defects, pin holes and thickness defects	25	Electrodes and wiring formation II	Mismatched alignments (mask alignments)
6	Gate formation (oxidized films)	Interfusion of foreign materials	26	Electrodes and wiring formation II	Interlayer connection sections (aspect ratios)
7	Gate formation (oxidized films)	Crystallization defect of silicon in lower layer of oxidized gate film (depth orientation)	27	Electrodes and wiring formation II	Interlayer connection sections (opening ratios)
8	Gate formation (electrodes)	Mismatched gate lengths	28	Electrodes and wiring formation II	Interlayer connection section defects (regardless of layer structures)
9	Gate formation (electrodes)	Structural abnormalities, voids and etching defects (overhangs)	29	Electrodes and wiring formation II	Crystallization defect of silicon in the lower layer of contacts
10	Gate formation (electrodes)	Interfusion of foreign materials	30	Electrodes and wiring formation II	Silicon nodule of contact section (single aluminum layer)
11	Gate formation (electrodes)	Mismatched alignments (mask alignments)	31	Electrodes and wiring formation II	Alloy spikes (single aluminum layer)
12	Interlayer dielectric film formation	Interfusion of foreign materials	32	Electrodes and wiring formation II	Voids and embedding defects (plug connections)
13	Interlayer dielectric film formation	Evenness abnormalities, thickness defects and coverage defects	33	Electrodes and wiring formation II	Structural abnormalities
14	Interlayer dielectric film formation	Voids	34	Electrodes and wiring formation II	Interfusion of foreign materials and contaminations (plug connections)
15	Interlayer dielectric film formation	Structural abnormalities	35	Protective film formation	Film thickness abnormalities (excluding organic protective films)
16	Electrodes and wiring formation I	Overall film thickness abnormalities	36	Protective film formation	Structural abnormalities
17	Electrodes and wiring formation I	Structural abnormalities and etching defects	37	Protective film formation	Cracks, chips, fractures and peelings
18	Electrodes and wiring formation I	Aluminum crystallization grain radius abnormalities (for single aluminum layers)	38	Protective film formation	Pin holes and voids
19	Electrodes and wiring formation I	Line breaks at stepped wiring segments (wire disconnection)	39	Protective film formation	Structural abnormalities
20	Electrodes and wiring formation I	Hillock 40	40	Protective film formation	Interfusion of foreign materials and contamination

Further, five is the minimum number of samples required for conducting an inspection for the purpose of process diagnosis, however, this is the absolute minimum number of samples that can be used for an investigation that involves conducting all inspection items. Although the number of subject samples is small, process diagnosis inspections are destructive inspections that require a lot of effort, thus a large volume of inspections cannot be expected.Since structural defects arising in wafer processes tend to occur in particular lots or particular lines and as the main purpose of the inspection is to rank electronic devices, a random spot inspection method involving a small number of samples is adopted.

Evaluation item of LSI process diagnosis

Data obtained from inspections on five inspection items are diagnosed and ranked according to the diagnosis standards, set with detailed descriptions for each of the 54 individual evaluation items intended for the process diagnosis as shown in Table 2. Specific defects found in each individual process are described in evaluation items and a quantitative evaluation and ranking is made possible by comparing these with non-conforming structures detected through inspections.

The diagnosis standard that becomes crucial to the process diagnosis is our own unique standard, which was derived from approximately 5,000 cases of failure analysis case examples from past experience, as well as conforming article analysis and various documented examples.

Detailed measurements from device structures are taken simultaneously in order to identify the design rules of electronic devices, along with the inspection of these evaluation items.

(1) Classifications of detected defects and demerit point categories

Risks of detected defects triggering failure with electronic devices vary in type, location and size of defect. Therefore, ranking is conducted using demerit categories, such as those described in Table 3. Although these demerit categories are also our own unique standards, similar to evaluation items, these have been derived from approximately 5,000 cases of failure analysis case examples from past experience, as well as conforming article analysis and various documented examples.

Table 3 Classifications of detected defects and demerit point categories.

Classification	Severity of defect	Condition	Demerit point category				Remarks
			A	B	C	D	
Ⅰ	Severe defect	Fatal	-1000	-	-	0	Great potential for inducing failure
Ⅱ	Moderate defect	Restrictive	-300	-200	-100	0	Moderate potential for inducing failure
Ⅲ	Slight defect	Hold	-30	-20	-10	0	Slight potential for inducing failure
Ⅳ	No classification		-	-	-	0	-

(2) Ranking electronic devices

Electronic devices subject to evaluation are assigned a rank from a six-step ranking system and determination results as shown in Table 4, based on the evaluations and rankings on the 54 items from five inspection items. Assigning ranks to electronic devices is conducted by a point reduction method with 1,000 points as the starting point. Demerit points are deducted from the original number of points, according to the demerit category based on the type, location and size of the defect. The distribution of results for ranking approximately 100 varieties of electronic devices, for which trial runs of LSI process diagnosis was conducted, is shown in Figure 2.

Table 4 Assigning ranks to electronic devices.

Ranking category	Assigned rank	Determination
Excellent	1000	Pass
Very good	751~999	
Good	501~750	
Passing	251~500	
Below averaging	1~250	Hold
Failure	0	Fail

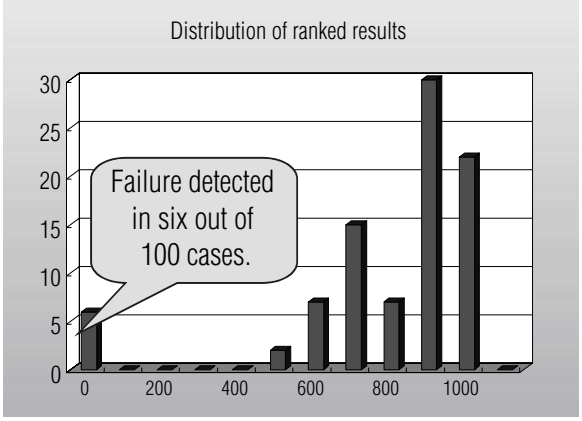

Fig. 2 Distribution of ranked results.

This figure represents a distribution of ranks based on the results of a diagnosis obtained from a database established for the purpose of LSI process diagnosis. The results according to this figure indicate that approximately six out of 100 cases have been detected with failures.

The database system of the LSI process diagnosis system allows for the extraction of structural values of electronic devices, such as the ranking distribution or wiring widths, based on arbitrary keys, such as the manufacturer, design rule, etc.

LSI process diagnosis database system

A large amount of diagnosis data is generated by the LSI process diagnosis, as 54 items are evaluated. An LSI process diagnosis database system has been constructed to make it possible to efficiently process and effectively utilize the diagnosis data. The LSI process diagnosis database system has been constructed with the Access database software of Microsoft and customized for process diagnosis to make its operations on personal computers possible out of a consideration for versatility. The appearance of an actual process diagnosis database is shown in Figure 3.

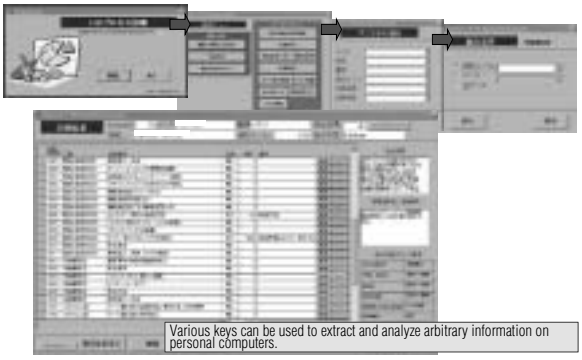

Fig. 3 LSI process diagnosis database system.

A large quantity of process diagnosis data is input into the database system to raise the quality of the LSI process diagnosis system through the accumulation of data with a high utility value that can be used for comparison and analysis.

Extraction of data is possible using items, such as those shown in Table 5, as part of the utility example of the database system. Although these are the results of rankings assigned for the products of each manufacturer and therefore, based on a unique ranking standard, it is possible to estimate the performance tendencies of individual manufacturers and individual process rules.

Table 5 Extraction examples from process diagnosis data.

Selection item	Classification	Selectable range
Manufacturer	Narrow down for each manufacturer	Individual manufacturer
Model	Individual model selection	Individual model
Type	Logic, memory, etc.	Nine items
Design rule	0.6 to 0.18 μm	Four steps
Diagnosis results	Ranks assigned based on ranking results	Seven steps
Diagnosis items	Individual defect item	54 items

Furthermore, detailed measurement values of the gate lengths, respective wiring widths, contact radius, aspect ratio of contact sections, coverage, etc., which are important structural values of electronic devices, have been entered to make it possible to extract and display data with arbitrary keys. A display example representing a display of the passivation film thickness is shown in Figure 4. Through such data analysis, it is possible to verify whether there is any discreteness with the structure of electronic devices, such as film thickness values or coverage values.

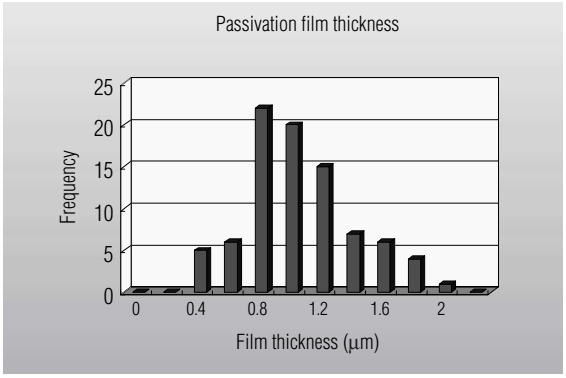

Fig. 4 Extraction example of device structure values.

Actual examples of LSI process diagnosis

(1) Actual example of detected non-conforming structure

Figure 5 shows a foreign material detected during an etch back inspection in the edge segment of relatively wide wiring inside an interlayer film.

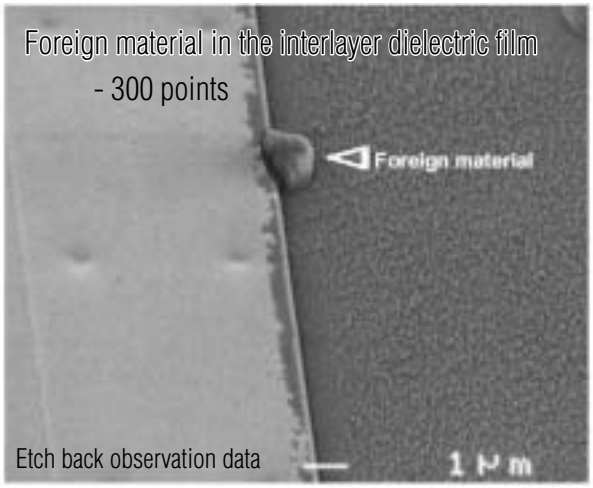

Fig. 5 A defect detected by etch back inspection.

These sorts of foreign materials vary in their impact on the electronic devices depending on the location detected and size, however, if they were located in a vital location, such as a contact, it would lead to a fatal defect. For this reason the detection of such foreign materials, even in areas where the impact on the electronic device is relatively small, such as the location shown in the figure, it is considered seriously and in these instances they are classified as moderate defects, which are subject to demerit points of -300.

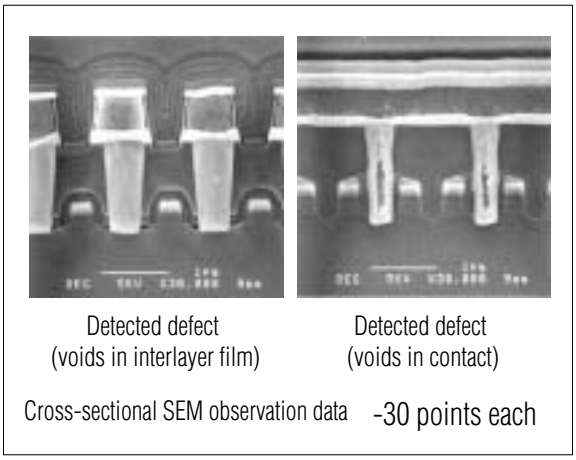

Fig. 6 Defects detected by cross-sectional SEM inspection.

Figure 6 shows voids inside a W-plug and voids in the interlayer film that were detected by a cross-sectional SEM inspection. Many such defects are seen with electronic devices (corresponding to 70% of the search results in the database), but the potential of these directly leading to a failure is relatively low and are therefore, classified as slight defects subject to -30 demerit points.

Figure 7 shows a crystallization defect in the silicon substrate that was detected by the cross-sectional TEM inspection. Since the size of the defect is larger than the cell size and since it is in the proximity of a channel, the potential of this leading to a failure is high and is therefore, classified as a severe defect subject to -1,000 demerit points. In such a case the ranking will be "Failure", however, since the location of the defect detection was in the cell block of a memory device, there is a possibility that this area could be processed as an unused block, so care is required when making determinations.

(2) Actual example of diagnosis results

An actual example of LSI process diagnosis results is shown in Table 6. This table shows the results obtained from a verification experiment on the process diagnosis and reliability test by obtaining two new lot samples for the two product types of A and B, which had in the past failed the LSI process diagnosis.

As a result of the diagnosis new defects were detected with one lot for each of the two product types A and B, which resulted in their failure. This diagnosis result indicates that there is potentially a problem with the quality of the manufacturing process for these two types of products.

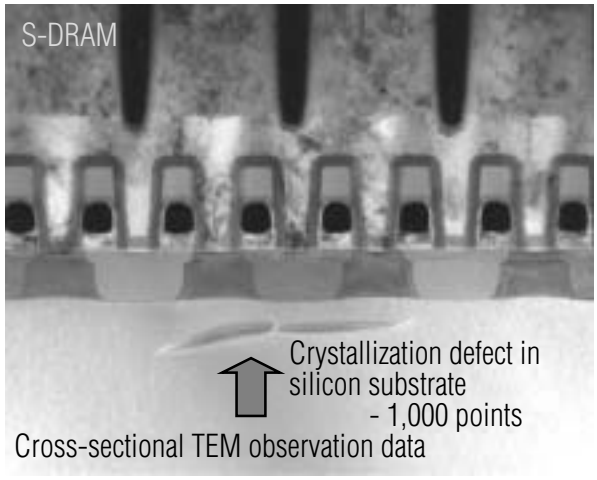

Fig. 7 Defects detected by cross-sectional TEM inspection.

Verification of LSI process diagnosis with reliability tests

The validity of selecting electronic devices through the method of LSI process diagnosis has been put under scrutiny with reliability tests[4].

Table 6 Example of LSI process diagnosis results.

Defect item No.	Defect item ID	Observation & evaluation items	Subject samples						Defect contents
			Samples No. 1			Samples No. 2			
			A	1	2	B	3	4	
1	B101	Wafer (separation of elements from substrate) & crystallization defects, pin holes, cracks and slips	0	-1000	0	0	0	0	Crystallization defect inside silicon substrate
2	B102	Wafer (separation of elements from substrate) & deformities and etching defects (bird's beak)	-100	-100	-100	0	0	0	Abnormal shape of STI structure
7	B203	Gate formation & crystallization defect of silicon in lower layer of oxidized gate film (depth orientation)	-30	-30	-30	-30	-30	-30	Residual transition in vicinity of gate edge segment
14	B303	Interlayer dielectric film formation & voids	0	-30	0	0	0	-60	(1) On the side surface of M1 (2) On the side surfaces of M1 and M2
21	B406	Electrode and wiring formation (wiring) & voids and scratches	0	0	0	0	-100	0	One location at M2
25	B502	Electrode and wiring formation (wiring) & mismatched alignment (mask alignments)	0	-300	0	0	0	0	Mismatched alignment with plug positioning between M1 and M2.
29	B506	Electrode and wiring formation (wiring) & crystallization defect of silicon in lower layer of contacts	-20	-30	-30	-20	-30	-30	Crystallization defect at lower segment of contacts
32	B509	Electrode and wiring formation (interlayer connections) & voids and embedding defects (for cases of plug connections)	-30	-30	-30	-1000	-30	-1000	(1) Silicon substrate contact segment (2) Connection interface of contact connection
43	B703	Memory cell segment & crystallization defect of memory cell segment	0	0	0	0	-30	-30	Crystallization defect of memory cell segment
47	B707	Memory cell segment & voids and embedding defects of contacts	-1000	-30	-30	0	-30	-30	Defective connection of pory-Si contacts
Overall determination		Demerit points	-1100	-1550	-220	-1050	-250	-1180	
		Ranking results	0	0	780	0	750	0	
		Ranks	FA	FA	VG	FA	GD	FA	

A high temperature operation test for 2,000 hours and a thermal shock test for 1,000 cycles were conducted on three lots of two product types from Table 6. As a result the occurrence of functional defects was verified in two out of 15 items from a single lot of one of the product types. The reliability test conditions are shown in Table 7. The product type (non-volatile memory listed under No. 2), for which the occurrences of functional defects were verified, was determined as a failure due to the defective connection of the W-plug as shown in Figure 8. Numerous defective connections of a similar kind were detected from the process diagnosis results (Figure 9), conducted following the reliability test, showed a rapid development of defective connections.

Table 7 Reliability test conditions.

Subject product type	Test code	Test conditions	Time of measurement (hours)	Test count	
				Classification	Count
No. 1	HTB	Failure determined through observation of DC, FCT, AC and MG at the initial test as well as periodical dynamic operation test with Ta=125˚C	Initial 168, 300, 500, 1,000 and 2,000.	Existing (A)	15
				New (1)	20
				New (2)	20
No. 2	HTB	Failure determined through observation of DC, FCT, AC and MG at the initial test as well as periodical dynamic operation test with Ta=125˚C	Initial 168, 300, 500, 1,000 and 2,000.	Existing (B)	15
				New (3)	20
				New (4)	20
	T/C	Failure determined through observation of DC, FCT, AC and MG at the initial test as well as periodical thermal shock test with Ta=55˚C to 125˚C	Initial 50, 100, 240, 500 and 1,000 (cycles).	Existing (A)	8
				New (1)	24
				New (2)	25

Further, the failure is determined to be from the defective connection of the W-plug based on the conditions of the defect mode (blanking time defect) as well. The leaning of the plug was also detected with products listed under No. 2 from the cross-sectional SEM inspection for products of other lots, although these have not reached a level of a failure in reliability tests. The defective connection of the W-plug, therefore, is thought to stem from a problem in the product process.

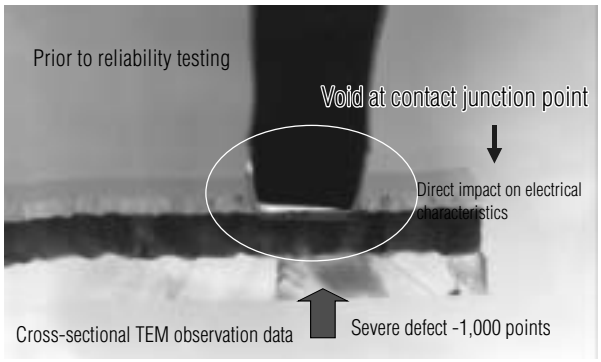

Fig. 8 Defective connection of W-plug listed under No. 2 - B.

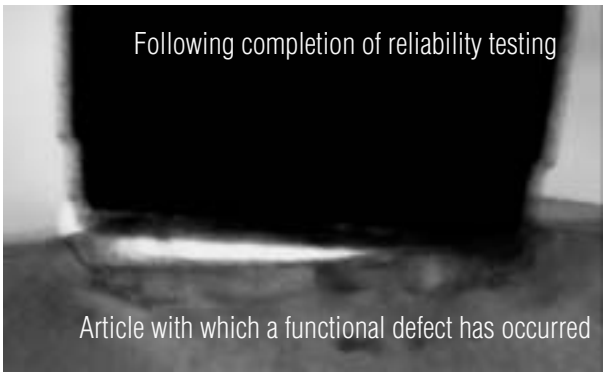

Fig. 9 Defective connection of W-plug listed under No. 2 - 1.

Non-conformities detected in the preliminary inspection varied between lots with products listed under No. 1 as shown in Table 6, while some of the non-conformities could not be detected during inspection after completion of the reliability tests, indicating that there is dispersion in quality among products of different lots. Although this is a problem related to product quality, no defects were detected during reliability tests. It is therefore, estimated that rapid development of defective factors could not be facilitated under test conditions.

The standard duration of ordinary reliability tests is 1,000 hours and therefore, the actual current situation indicates that those electronic devices with such inherent defective structures pass reliability tests and are distributed in the market.

Selecting electronic devices based on the LSI process diagnosis method is considered an effective means to prevent the danger of adopting such electronic devices for systems requiring a high degree of reliability

Conclusion

Since the LSI process diagnosis method is an evaluation of the wafer process itself it is possible to establish a more complete reliability evaluation system for systems requiring a high degree of reliability by combining it with the conventional reliability test and DPA for the assembly process itself.

Unlike failure analysis performed after a failure occurs the process diagnosis method, which analyzes conforming products, can be conducted immediately making it possible to eliminate defects in the early stages of a project without having to wait for the results of reliability tests that can take a lot of time and money. Further, even more complete and effective reliability tests can also be planned by implementing a process diagnosis in advance.

Data obtained from process diagnosis is entered into a database on the condition that it can be used in a systematic manner, making it possible for users to accumulate information regarding the wafer process.

This means that the PDCA cycle (Plan - Do - Check - Action) of the users can be accelerated, which is hoped to lead to the development of superior products and improvement in competitiveness.

References

1) Imai, et al: Issue R97-8 of Journal of IEICE, The Institute of Electronics, Information and Communication Engineers, September 1997.
2) Yoshida: The Thirteenth Symposium on Reliability and Maintainability, Union of Japanese Scientists and Engineers
3) Imai et al: SC-11-2 of the General Meeting, The Institute of Electronics, Information and Communication Engineers, March 1998.
4) Yabe et al: The Fourteenth Reliability Center for Electronic Components of Japan (RCJ) Reliability Symposium, November 2004.

Authors

Kazuhiro Yabe: Oki Engineering Co., Ltd., Reliability Engineering Div.
Daiki Tanaka: Oki Engineering Co., Ltd., Reliability Engineering Div.
Katufumi Noda: Oki Engineering Co., Ltd., Reliability Engineering Div.
Sadao Suganuma: Oki Engineering Co., Ltd., Reliability Engineering Div.
Katsumi Oka: Japan Aerospace Exploration Agency (JAXA)
Satoshi Kuboyama: Japan Aerospace Exploration Agency (JAXA)
Sumio Matsuda: Japan Aerospace Exploration Agency (JAXA)

This report was taken from the published papers at the 34th Symposium on Reliability and Maintainability by the Union of Japanese Scientists and Engineers and edited for reprint in this issue of the Oki Technical Review with the consent of the Union of Japanese Scientists and Engineers.