High-speed Color Printer Controller Hardware

Osamu Ishikawa Shoichi Ii

In recent years, as digital cameras and the Internet have become more widespread, the adoption of color in the office has increased rapidly and penetrated deeply. Receiving presentation materials printed in color is no longer a rare event. The market therefore requires color printing to be fast and easy. To achieve higher printing speeds, Oki Data offers high-speed color printers using the Single Pass Color® *1) method (tandem type). The controller that generates the image data that brings out the full capability of Single Pass Color® printing, which simultaneously prints the four colors Y (yellow), M (magenta), C (cyan), and K (black), must handle each color appropriately. Also, since it handles all four colors simultaneously, the controller must have approximately four times the data handling capacity of controllers that overlay the four colors in series.

This article introduces the trends in color printer controller hardware and provides an overview of the Single Pass Color® type color printer controller hardware that Oki Data provides from the viewpoint of both high-end controllers and low-end controllers.[1) 2)]

Trends in the Color Printer Controller Market

(1) Tandem type and 4-Pass type

Four-Pass type printers sequentially print each color in the order Y → M → C → K, so the controller only needs the capacity to handle the data for one color at a time. On the other hand, since tandem type printers print all four colors simultaneously, the controller has to process the data for all four colors at the same time. Because controllers process data using mainly the CPU, the operating frequency of the CPU is considered one index for measuring the performance (processing capacity) of the controller. Other indices are the memory bandwidth that expresses the data access capacity between CPU and memory, image processing achievable by the ASIC, and the interface reception capacity.

Fig. 1 is a plot of the relationship between the CPU operating frequency and color printing speed of printers recently announced by each manufacturer. The printers are grouped into the tandem type and the 4-pass type. The 4-pass printers announced to date are concentrated in the slow printing speed area. Nearly all of the fast printers are tandem type printers. In addition, it is clear from Fig. 1 that the operating frequency of CPUs used in tandem type printers is higher than that of CPUs used in 4-pass printers. It is also clear that the operating frequency of the CPU used tends to increase as the printing speed increases.

*1) Single Pass Color is a registered trademark of Oki Data Corp.

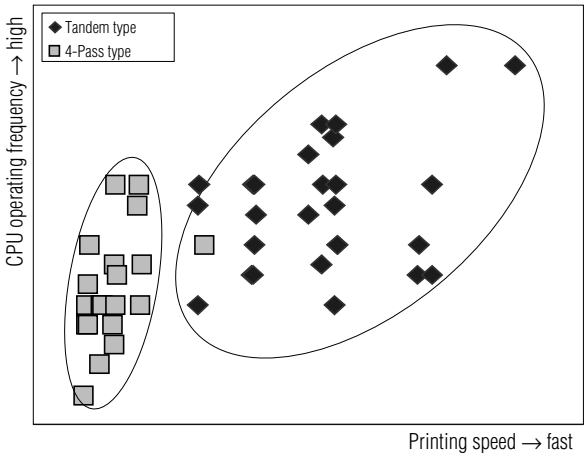

Fig. 1 Relationship Between Printing Method, CPU Operating Frequency and Printing Speed

(2) Relationship between printing language type and controller

Printers receive from a PC or other host computer printing data described in a page description language (PDL) such as PostScript or PCL, convert it into bitmap data, then print. Performing the work of converting this printing data into bitmap data is the main function of the controller, so performance of the controller is also heavily dependent on performing the conversion work at high speed. In this regard, CPUs with an operating frequency exceeding 3 GHz are being announced for use in PCs, etc., so an improvement can be seen in the processing capacity of PCs. As this operating environment changes, host-based color page printers are also being announced where the host computer performs the work of converting printing data into bitmap data, sends the generated bitmap data to the printer, and then the printer prints the bitmap data as it receives it. Since the printer does not perform conversion tasks that require high performance, it is possible to simplify the printer controller and realize lower cost relatively easily.

Fig. 2 classifies the relationships in Fig. 1 into “host-based printers” and printers that use page description language. Since the controllers are not required to have high performance, it is clear that host-based printers use CPUs with low operating frequencies. This is even the case for printers with the same printing speed.

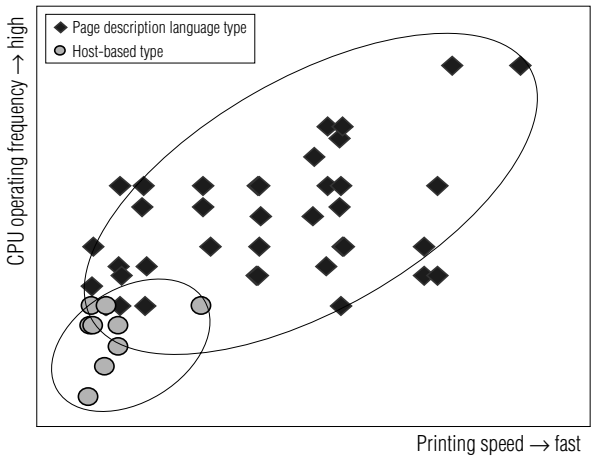

Fig. 2 Relationship Between Printing Language Type, CPU Operating Frequency and Printing Speed

Introduction of High-end Color Printer Controller Hardware

(1) An overview of high-end color printer controllers

High-end color printers that achieve speed and high resolution use page description language to remain independent and not place a load on the host computer. These printers receive printing data described in page description language from the interface, perform editing or expanding processes according to this data, and then generate the bitmap data for the colors Y, M, C and K simultaneously. In editing processes, these printers convert the printing data into a format that is easy to expand, then generate intermediate data. In expansion processing, these printers perform processing such as overwriting the intermediate data as bitmap data, which functions as plotting instructions, and then generate the final bitmap data. This series of processes requires the most CPU power. The reason that CPUs with high operating frequencies are used is to perform these processes at high speed. On the other hand, the processing content of binary processes such as compression/decompression, color conversion, or dither has relatively simple algorithms, so they are often handled using ASICs. Functions performed using ASICs can achieve processing speeds several times that of processing done using CPUs.

(2) Configuration of high-end color printer controllers

Fig. 3 is a functional block diagram of high-end color printer controller hardware. In order to enable large-volume data accessing, without interruption, through memory accessing from the CPU or from an image processing module implemented as an ASIC, ASIC internal busses and SDRAM controllers are being developed. Also, to make it possible to access Program ROM which stores CPU instructions and to access SDRAM in parallel, separate data busses for Program ROM and for the SDRAM were established. For the image processing function performed by the ASIC and the video output block that outputs bitmap data to the engine controller, we carefully studied and evaluated the processing capacity and circuit scale and, where necessary, built multiple circuits. In regard to the CPU, we took account of operating frequency, cache size, the capacity of the FSB (Front Side Bus) which performs data access to external elements and the fact that the CPU processing load is lightened due to the functions performed by the ASIC. Based on that, we selected and specified a CPU which would enable maximum performance of the system to be achieved. As for the interfaces, we implemented 10Base-T/100Base-Tx, USB, and IEEE1284 interfaces, enhancing the system's adaptablility to the operating environments. It is also important to offer wireless LAN and Gigabit Ethernet such as IEEE1394 or IEEE 802.11a/b/g to meet market needs.

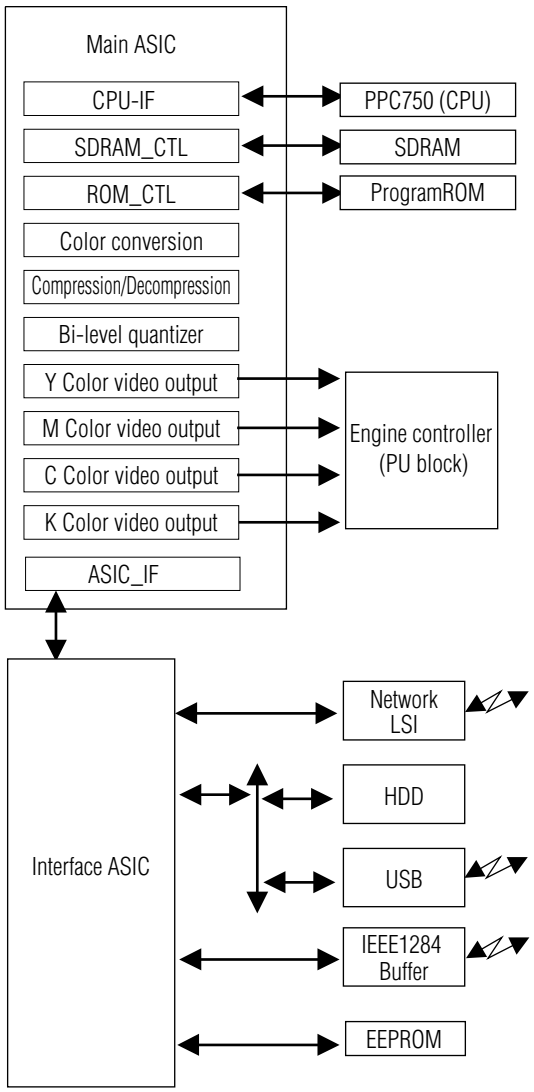

Fig. 3 High-end Color Printer Function Block Diagram

Data transfer speeds of 100 MHz or more between the CPU and ASIC or ASIC and SDRAM are starting to be realized, and the layout of wire patterns on the boards on which the CPU, ASIC, etc. are mounted is becoming important technology. Before determining the ASIC pin placement or I/O buffer type, it is necessary to route virtual wire patterns, select the optimal pin placement or I/O buffer type in a board simulation using the IBIS (I/O Buffer Information Specification) model, and sufficiently study the layout of the wire pattern. In the future printer market, high-speed serial busses such as PCI Express™*2), HyperTransport™*3), or RapidIO™*4) may become more widespread, so a technology will be required that can realize on-board transfer speeds of several hundred MHz to several GHz.

Introduction of Low-end Color Printer Controller Hardware

(1) An Overview of low-end color printer controllers

Low-end color printers that realize high speed and low cost are host-based type printers wherein a PC converts printing data into bitmap data. With this type of printer, the printer driver that runs on the PC generates Y, M, C and K bitmap data, compresses the data, then sends the data to the printer. On the other hand, the controller receives the data from the interface, decompresses the data, restores the Y, M, C and K bitmap data, then prints the data. In this way, assigning the creation of bitmap data, which is the process requiring the most CPU power, to the PC makes it possible to use an inexpensive CPU. The performance of this type of controller is determined by reception performance and expansion performance.

(2) Configuration of low-end color printer controllers

Fig. 4 is a functional block diagram of low-end color printer controller hardware.

In order to reduce costs, these controllers consolidate functions onto a single ASIC and reduce the number of components. Compared with the ASIC used in high-end controllers, this ASIC reduces the number of external pins by sharing a data bus for SDRAM, Network LSI, and USB LSI, and by reducing the bus width (changing to 32 bits). The interfaces emphasize reception performance and incorporate High Speed USB2.0, in addition to 10Base-T/100Base-TX, instead of mounting a low-speed IEEE1284 interface. For the algorithms that compress/decompress the data received from the PC, we adopted JBIG, which uses highly efficient compression. By combining it with a high-speed interface, it is possible to receive and process the bitmap data created by the PC at high speed. The LED head control circuits that existed in previous engine controllers (PU blocks) were realized by a dedicated ASIC. However, as shown by the LED_CTL module in Figure 4, we were able to reduce cost by integrating all functions into a single ASIC and reducing the number of components.

As a way to further improve performance, using hardware to perform network processing and decompression processing is also being considered, in addition to making the ASICs faster. However, making ASICs faster sometimes leads to higher ASIC cost. In the case of low-end printer controllers, we consider it very important to adapt the design to the speed of the printer engine. LED head control circuits are already being incorporated as a means of lowering costs, but incorporating CPUs and motor control circuits for the PU side are the current issues.

With host-based printers, it is better if the PC performance is high, and there are cases if PC performance is too low, it becomes unsuitable. Consequently, figuring out how to achieve controllers that can execute page description language at a cost similar to that of host-based printers is the current topic.

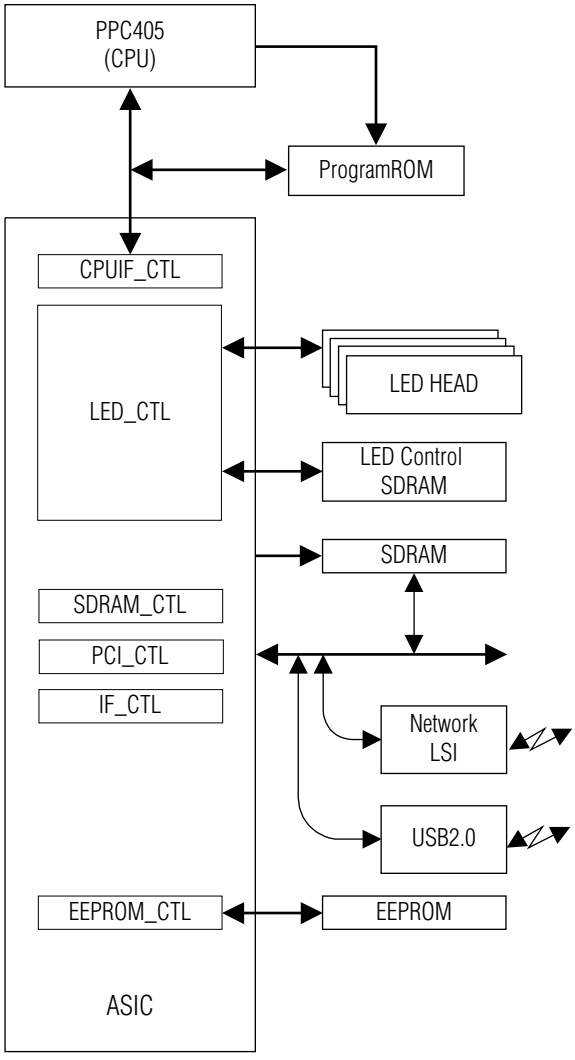

Fig. 4 Functional Block Diagram of Low-end Color Printers

*2) PCIExpress is a trademark of PCI-SIG.
*3) HyperTransport is a trademark of the HyperTransport Technology Consortium.
*4) RapidIO is a trademark of the RapidIO Trade Association.

The Future of Color Printer Controller Hardware

Color printers will continue to become faster and deliver even higher resolution, and it is expected that image processing functions of even greater sophistication will also be required. Therefore, even more advanced performance will be demanded of controller hardware. At the same time, the market will demand lower cost and greater ease of use. It then becomes important to provide controller hardware that satisfies these demands and maintains a fine balance between performance and cost.

(1) Pursuing faster speed

The main factors impacting controller performance are the CPU, memory, and ASIC. In particular, it is not an overstatement to say that the interface with the CPU, the interface with memory, and the ASIC functions that accomplish image processing determine the controller's overall performance.

CPUs are often evaluated by the performance index of their operating frequency. However, the bandwidth capacity of the FSB that CPUs use to access the outside is important, and it is necessary to develop ASICs that support fast FSBs operating at several GByte/sec to improve the performance of the CPU factor. Improving the bandwidth capacity of FSBs makes it possible to increase the ratio at which improved CPU operating frequency contributes to performance.

It is necessary to improve the FSB bandwidth capacity of the CPU while improving the bandwidth capacity of memory as well. We must also develop ASICs that incorporate memory controllers that realize memory bandwidth of several GByte/sec in the DDR (Double Data Rate)-SDRAM currently used in PCs or its expected successor DDR-II.

(2) Pursuing lower cost

Controller cost can be broken down into CPU, ASIC, RAM such as SDRAM, Program ROM, and interfaces (in particular, network interfaces). Of these factors, the CPU and ASIC costs account for a large portion of the controller cost. Reducing the costs of CPUs and ASICs in low-end controllers is an important topic.

In recent years, semiconductor processes have advanced considerably and it is becoming possible to realize ASICs with several Mgates. We must consider lowering costs by realizing on a single ASIC those functions that were previously implemented on separate ASICs. Another promising avenue is incorporating CPUs into ASICs.

This article described fast color printer controllers from the viewpoint of hardware. In order to offer fast color printer products that are faster and more convenient to use, we will work towards developing controller hardware that has high performance and low cost.

References

1) Masato Nagata, Yoshitaka Nishiyama, Kazuhiko Ito: Oki Technical Review 185, Fast Controller Technology of Single Pass Color™ Printers, Vol. 68 No. 1, pp. 128-131, January 2001.
2) Eiji Ishikawa, Nobuhiro Yoshida, Masato Nagata, Masahiro Yoshimoto, Susumu Sato: Oki Technical Review 178, Color Electronic Photograph Printer Control Technology, Vol. 65 No. 2, pp. 23-28, May 1998.

Authors

Osamu Ishikawa: Oki Data Corp., Controller Development Center, Hardware Development Dept., General Manager

Shoichi Ii: Oki Data Corp., Controller Development Center, Hardware Development Dept., Team Leader