Fully-depleted Type SOI Device Enabling an Ultra Low-power Solar Radio Wristwatch

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On May 19, 2002, Casio Computer Co., Ltd. launched sales of the Tool Concept PRG-50, a new addition to its Pro Trek series of "outdoor" watches which provide compass direction and altitude readings. Moreover, these watches run on solar power, so there is no need to worry about battery replacement. (See Fig. 1.)

The Tool Concept PRG-50 employs a low-power LSI IC designed for watches which includes an Oki Electric fully-depleted type SOI (Silicon-On-Insulator) CMOS device (FDSOI-CMOS) [1] [2] [3] for greatly reduced current consumption. Thanks to the high-performance solar drive system built into this chip, plus a solar panel that provides highly efficient power generation and a high-storage-capacity battery, this watch is able to use solar power to operate direction and altitude functions-features not found in conventional solar watches. As such, the Tool Concept PRG-50 is a high-performance outdoor watch that hikers and trekkers can trust, without any worries about low batteries.

The following [4] describes how the fully-depleted type SOI CMOS device (FDSOI-CMOS) was developed for Casio for use as a watch-type LSI IC (product name: ML6126) that boasts the world's lowest current consumption.

Fig. 1   Tool Concept PRG-50

Reducing Current Consumption in LSI ICs for Watches

The push for lower current consumption in Casio's LSI ICs for watches began in earnest around 1997. In addition to meeting the needs for longer watch battery life and reduced environmental impact, Casio was seeking to use thinner button-type batteries to power their watches. Using these button batteries would enable the watch

itself to be made thinner and more fashionable.

Conventional IC chips for watches, such as the MSM6118, were rated (in chip-specific electrical characteristics) to consume 1.55 μA of current. Since 1997, current consumption has been successively reduced by circuit design measures, use of the multiple threshold value process, and layout techniques scaled to 1.3 μA (in the MSM6121), then to 0.7 μA (in the MSM6122). (The multiple threshold value process uses at least two different threshold values. Transistors that require only the lower threshold value are designed to use that lower value while other transistors use the higher threshold value, which enables both low leakage current and low-voltage operation.)

In the MSM6122, when the threshold value is at the center of the target value range, the chip's actual current consumption is raised to 0.33 μA, and when the threshold value is at the worst level, the leakage current is increased such that the current rating becomes 0.7 μA. At the same time, even when the threshold value is at the center of the target value range, the charge/discharge current for the crystal oscillator circuit, main clock circuit, and display circuits made it difficult to reduce current consumption. Consequently, an FDSOI-CMOS process using fully-depleted type SOI was adopted as a solution for reducing current consumption.

Advantages of the FDSOI-CMOS Process

Listed below are some of the advantages of using the FDSOI-CMOS process as a means of reducing current consumption in LSI ICs for watches.

① Low parasitic capacitance

② The threshold voltage can be set lower than in bulk devices.

These advantages are further described below.

The junction capacitance that is a component of a MOS transistor's parasitic capacitance is proportional to the junction surface area, and the junction surface area is the sum of the plane and lateral surface areas of the source/drain diffusion layer. In FDSOI-CMOS devices, the bottom surface is connected to a thick oxide film (embedded oxide film), which greatly reduces capacitance [5]. As for the lateral areas, only the parts that face channels are affected, and the overall capacitance is reduced to about one tenth that of the source/drain junction area in conventional bulk devices. Accordingly, the capacitance subject to load charges and discharges is reduced, making for lower current consumption. For example, charge/discharge current for the watch's LCD driver block, step-up, and step-down circuits can be

reduced to 30 nA to achieve lower current consumption.

One of the chief features of FDSOI-MOS devices are their sharp sub threshold characteristics. The S factor value, which indicates the amount of gate voltage required to effect an order of magnitude change in the sub threshold voltage can be expressed as follows.

$$S = (1 + \frac{C_d}{C_{ox}}) \frac{kT}{q} \ln(10) \quad \text{(Equation 1)}$$

where C_d is the channel's depletion layer capacitance, C_{ox} is the gate capacitance, k is Boltzmann's constant, T is the absolute temperature, and q is the charge.

In an FDSOI device, elements are formed on a buried oxide film, so:

$$C_d = \frac{\varepsilon_{Si}}{t_{Si}} / \left(\frac{\varepsilon_{Si}}{t_{Si}} + C_{BOX} \right) \quad \text{(Equation 2)}$$

can be expressed. Here, ε_{Si} is the silicon permittivity, t_{Si} is the SOI film thickness, C_{BOX} is the buried oxide film capacitance, which can be reduced relative to bulk devices where ε_{Si} / l_d (l_d being the depletion layer width). Accordingly, the S factor value can be lowered to 60 to 65 mV/dec in SOI-MOS devices, compared to 80 to 95 mV/dec in bulk MOS devices [5].

As a result, an FDSOI device with equivalent OFF leakage current can be set with a much lower threshold voltage than is possible in bulk devices. While bulk devices required two power sources-one for logic circuits and the other for the oscillator circuit-the logic block in FDSOI-MOS devices can operate at a lower voltage so that only one power source is needed. Circuits that employ these characteristics are shown in Figs. 2-1 and 2-2.

Fig. 2-1 shows part of the power supply configuration in the ML6122 (0.5-μm bulk process). After the battery power is reduced by half by a step-down transformer circuit, it is supplied from two regulator circuits to various microprocessor blocks (ROM, RAM, CPU, etc.) and to the crystal oscillator circuit.

The threshold values of the PMOS and NMOS transistors in the microprocessor blocks are set to -1.0 V and 0.7 V respectively. These values are set so as not to increase the OFF leakage current within the process variation range. In such cases, the minimum operating voltage of the microprocessor blocks depends on the greater of two absolute values-the PMOS threshold value and the NMOS threshold value. Accordingly, the optimum voltage supplied from the regulators to these microprocessor blocks is approximately 1.1 V.
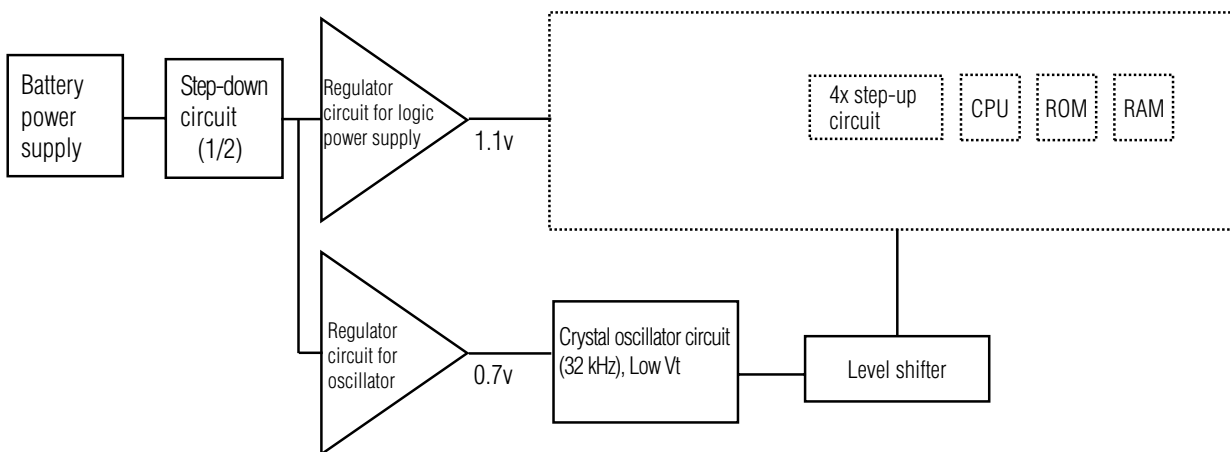

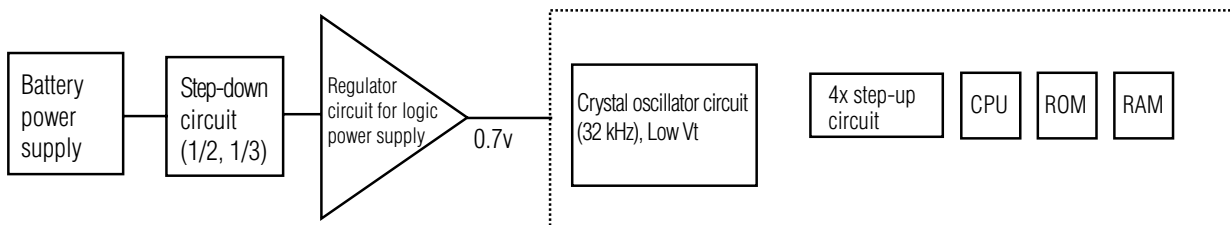Fig. 2-1. ML6122 Logic Power Supply Configuration (0.5 μm process bulk CMOS)

Fig. 2-2. ML6126 Logic Power Supply Configuration (0.35 μm process SOI)

Fig. 2 Comparison of Power Supply Configurations in Bulk Process and SOI Process

In addition, the threshold values of the PMOS and NMOS transistors in the oscillator circuit are set to -0.35 V and 0.35 V respectively. The purpose of this is to enable oscillation to be maintained even though the oscillator circuit has a low supply voltage. It also serves the purpose of reducing the oscillator circuit's own current consumption. In this case, the oscillator circuit's minimum operating voltage depends on the voltage which is added to the absolute values for PMOS threshold value and NMOS threshold value. Consequently, the optimum voltage supplied from the regulator to the oscillator circuit is approximately 0.7 V.

Fig. 2-2 shows the power supply configuration used for the FDSOI-CMOS process. The reduction of the S value and the migration from a 0.5-mm process to a 0.35-mm process (both advantages of SOI) narrows the total gate width inside the microprocessor block, which has enabled a lower threshold voltage than is possible in bulk devices. The threshold value was finely adjusted in 10-mV units to optimize it so that the microprocessor circuits are able to operate with a minimum operating voltage of about 0.7 V. In addition, the threshold value of the oscillator circuit was also finely adjusted and optimized so that the oscillator circuit and microprocessor block could operate using the same voltage.

This power supply configuration enabled current to be reduced in the level shifter circuit and logic power supply regulator circuit, and also enabled reduction of the charge / discharge current within the microprocessor block. The total current reduction effect came to 100 nA.

As described above, this adoption of the FDSOI-MOS process allowed a 40% reduction in current consumption.

Disadvantages of SOI Process and Measures to Deal with them

The disadvantages of the SOI process for watch LSI ICs include the following.
① Low element withstand voltage.
② Low ESD (electrostatic discharge) tolerance. (ESD tolerance is the ability to avoid damage by tolerating exposure to electrostatic charges such as ESD emanating from human bodies or component packages into the LSI IC.)

For practical purposes, the element withstand voltage of the 0.35-mm FDSOI-MOS process used in this watch LSI IC is 1.5 V. When 1.5 V or more is applied between an element's source and drain, the current between the source and drain increases due to parasitic bipolar operation.

Since the maximum power supply voltage for this IC is 3.4 V, in a bulk CMOS device where the source-drain voltage is at least 6 V, the current would increase and problems such as operation faults in analog circuits would occur, so countermeasures would be needed. These countermeasures are described below.

Low-voltage operation of microprocessor block

The device was designed so that a power supply voltage of at least 1.5 V would not be applied, so as to enable all circuits other than those required by external and interface circuits to be driven by the output voltage of the regulator circuits.

Higher withstand voltage of external interface circuits

Since 3.4 V is applied to the digital circuits that are required for external and interface circuits, a two-layer PMOS configuration and three-layer NMOS configuration are used, as is shown in Figure 3. This enables the source-drain voltage applied to each transistor layer to be lowered, which avoids any increased current caused by parasitic bipolar operation.
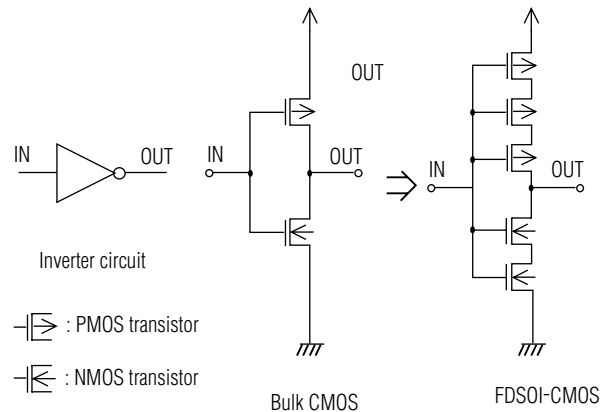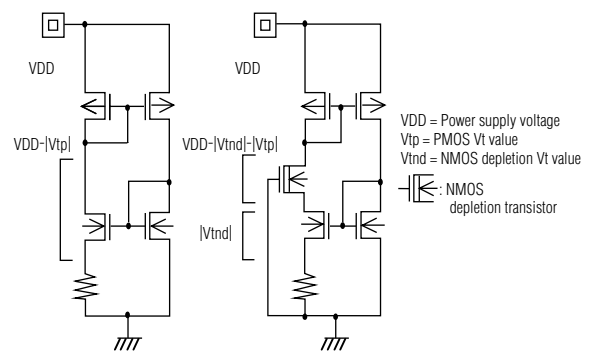

Fig. 3 Example of External Interface Circuit

Higher withstand voltage of analog circuits

In analog circuits, which must be driven by a power supply voltage in the range from 1.3 V to 3.4 V, a configuration of operation points was devised, with elements such as depletion transistors used to prevent the applied voltage from exceeding 1.5 V between source and drain in each circuit. An example of this is shown in Fig. 4.

Effect of circuit countermeasures: Circuit's minimum operating voltage was maintained and withstand voltage of | Vtnd | block circuits was increased.

Fig. 4 Example of Analog Circuit

Layout for higher withstand voltage

As a measure to increase withstand voltage of analog circuits, source tie type transistors have been used to fix the body potential for elements where voltage exceeding 1.5 V is applied. These source tie type transistors fix the body block to the source potential to suppress parasitic bipolar operation and to raise the withstand voltage. A layout diagram of source tie type transistors is shown in Fig. 5.
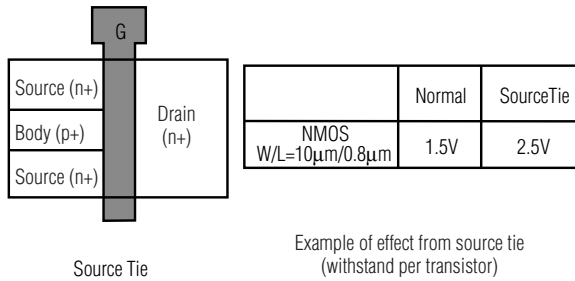

		Normal	SourceTie
NMOS W/L=10μm/0.8μm		1.5V	2.5V

Source Tie

Example of effect from source tie (withstand per transistor)

Fig. 5 Higher Withstand Voltage by Fixing of Body Potential

Fig. 6 shows the characteristics of a voltage regulator that employs both circuitry and layout-based countermeasures against high withstand voltage. Before these countermeasures were implemented, whenever the power supply voltage became high it increased the regulator's output voltage, which made it impossible to meet the user-specified rating. After these countermeasures were implemented, flat output characteristics were achieved (almost independent of the power supply voltage) thereby meeting the user-specified rating.

With regard to ESD, unlike with bulk CMOS process, only protective transistors are used at locations where ESD surges are to be avoided since there are no junctions in the board or well directions.

Consequently, the ESD tolerance of ML6126 is low compared to other bulk CMOS products. The issue of ESD protection for FDSOI-CMOS devices should be addressed by ongoing improvement efforts.
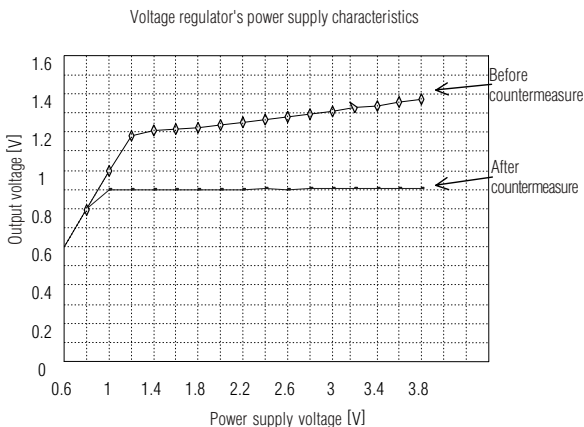

Voltage regulator's power supply characteristics

Fig. 6 Effects of Higher Withstand Voltage

Conclusion

Current consumption of the ML6126 was reduced to approximately 150 nA (Typ.) by using the FDSOI-CMOS process. This represents a reduction to one-eighth the current consumption levels achieved just a few years earlier.

In the future, FDSOI-CMOS will undoubtedly become the main process used in low-power LSI ICs such as those used in Casio's watches.

At present, the shift to full production has been completed for the ML6130, a successor to the ML6126 that uses this same process. In addition, the ML6190, an LSI IC that includes a radio reception function, is now in trial production and will later be added to this growing product line.

The dramatic reduction in current consumption that can be achieved using FDSOI-CMOS chips opens the door to a wide range of applications in addition to low-power watch LSI ICs. Major reductions in parasitic capacitance and the trend toward low-voltage threshold values promise to result in faster and faster chips as development is carried forward into the future. We at Oki Electric are looking forward to creating a number of products that will take advantage of FDSOI-CMOS features.

■ **References**

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